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Trends in e-beam Metrology and Inspection

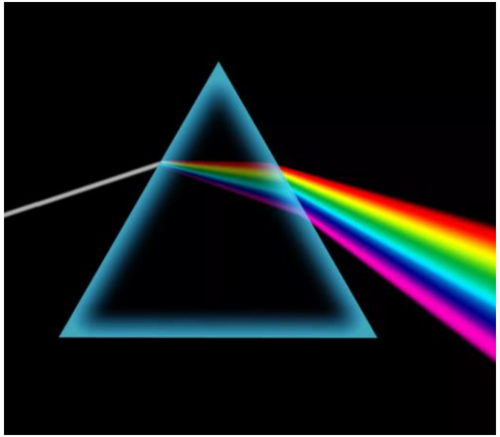
Gian Francesco Lorusso

Outline

- Introduction
  - Low Voltage
  - High Voltage
  - Backscattered
  - High Beam Current
  - AI
  - Multi-beam
- Conclusion

Introduction

INTRODUCTION: E-BEAM HISTORY

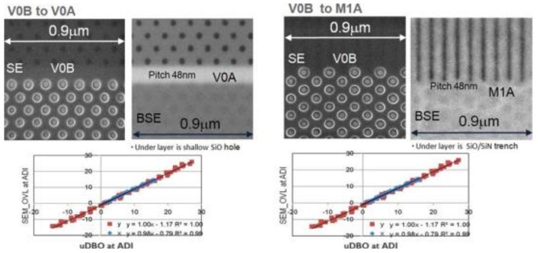


Classical CDSEM Age | Dark Age of Optical | *Electron Renaissance*

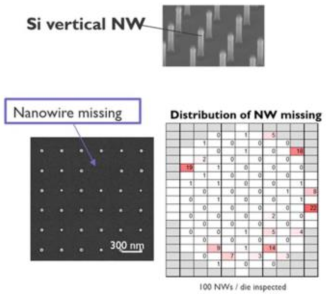
1980 | 2000 | 2020

Early signs of e-beam Renaissance

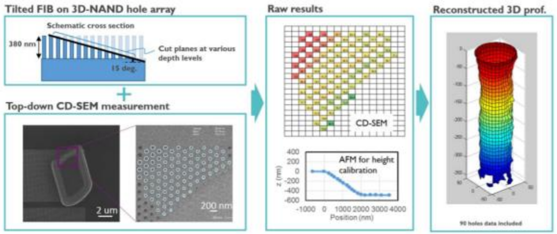
GF Lorusso, et al, "Enabling CD SEM metrology for 5nm technology node and beyond" Proc 10145: Metrology, Inspection, and Process Control for Microlithography XXXI SPIE (2017)



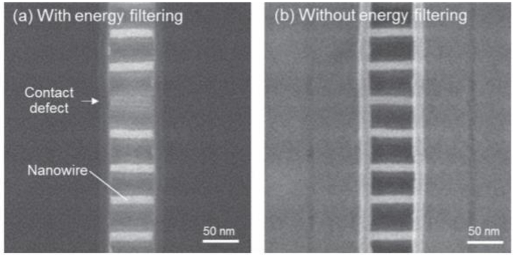
OVERLAY



DEFECTIVITY VERTICAL NW



3D RECONSTRUCTION

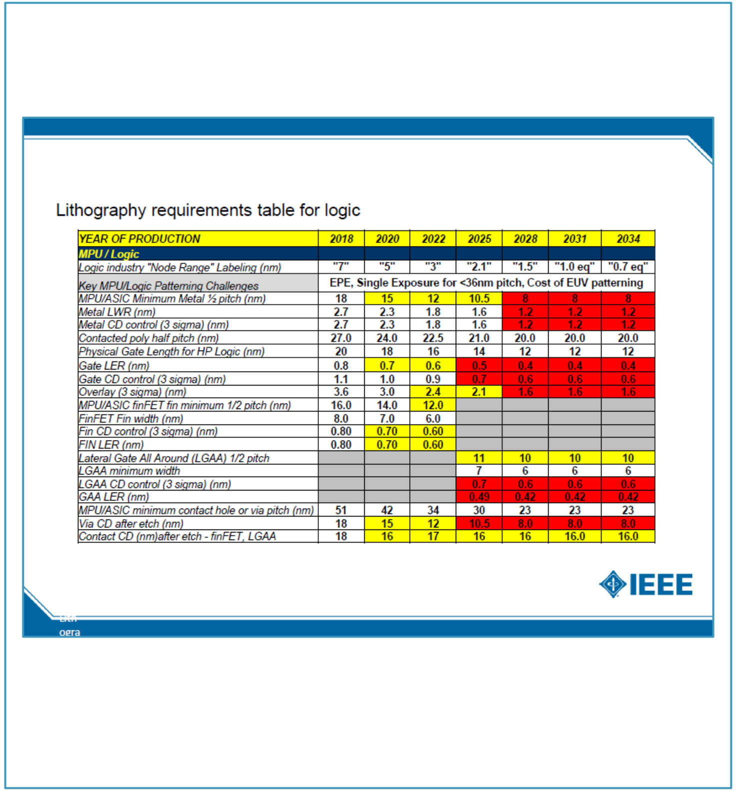


VOLTAGE CONTRAST LATERAL NW

Already in 2017, many "unconventional" CDSEM methods had started to appear

Factors driving Evolution

Mark Neisser, INC Conference (2020)



Lithography requirements table for logic

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
Key MPU/Logic Patterning Challenges	EPE, Single Exposure for <36nm pitch, Cost of EUV patterning						
MPU/ASIC Minimum Metal ½ pitch (nm)	18	15	12	10.5	8	8	8
Metal LWR (nm)	2.7	2.3	1.8	1.6	1.2	1.2	1.2
Metal CD control (3 sigma) (nm)	2.7	2.3	1.8	1.6	1.2	1.2	1.2
Contacted poly half pitch (nm)	27.0	24.0	22.5	21.0	20.0	20.0	20.0
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Gate LER (nm)	0.8	0.7	0.6	0.5	0.4	0.4	0.4
Gate CD control (3 sigma) (nm)	1.1	1.0	0.9	0.7	0.6	0.6	0.6
Overlay (3 sigma) (nm)	3.6	3.0	2.4	2.1	1.6	1.6	1.6
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0	12.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
Fin CD control (3 sigma) (nm)	0.80	0.70	0.60				
FIN LER (nm)	0.80	0.70	0.60				
Lateral Gate All Around (LGAA) 1/2 pitch				11	10	10	10
LGAA minimum width				7	6	6	6
LGAA CD control (3 sigma) (nm)				0.7	0.6	0.6	0.6
GAA LER (nm)				0.49	0.42	0.42	0.42
MPU/ASIC minimum contact hole or via pitch (nm)	51	42	34	30	23	23	23
Via CD after etch (nm)	18	15	12	10.5	8.0	8.0	8.0
Contact CD (nm)after etch - finFET, LGAA	18	16	17	16	16	16.0	16.0

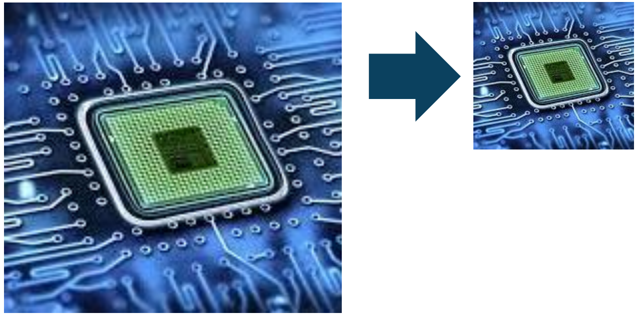
Imec-based e-beam tools

Factory-based e-beam tools

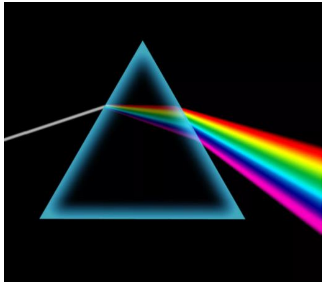
- High NA EUVL and new devices architectures are imposing requirements stricter than ever
- Imec engagement with all major e-beam equipment suppliers is a unique advantage

Low Voltage

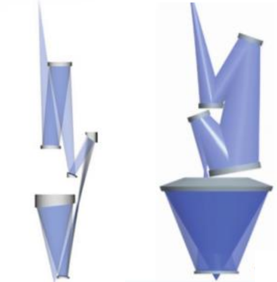
Why do we need thin resist?



Wavelength Scaling



NA Scaling



Rayleigh Resolution

$$CD = k_1 \frac{\lambda}{NA}$$

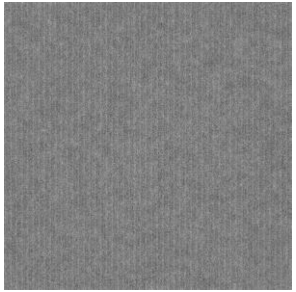
Rayleigh DOF

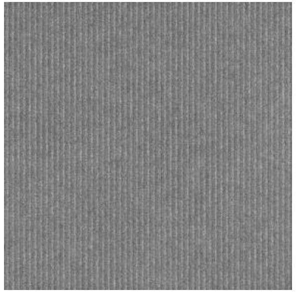
$$DOF = k_2 \frac{\lambda}{NA^2}$$

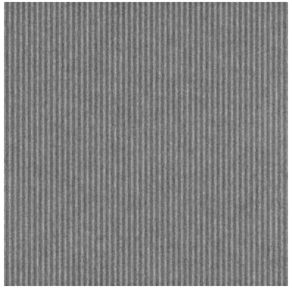
Thin resist is needed to cope with low DOF and to limit aspect ratios in High NA EUV

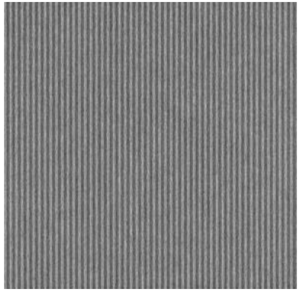
Baseline

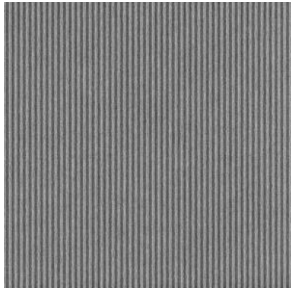
32nm LS

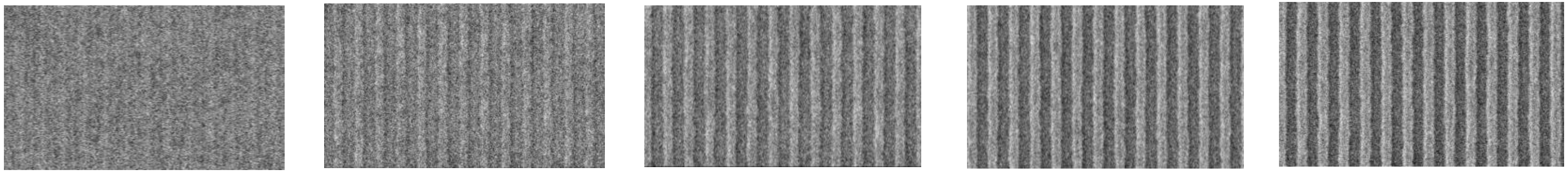

Target FT = 10nm


Target FT = 15nm


Target FT = 20nm


Target FT = 25nm


Target FT = 30nm



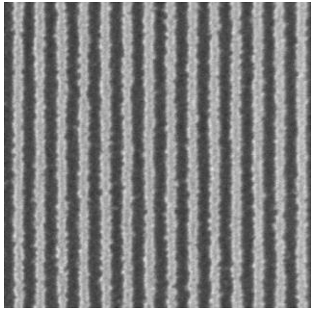
- Thinner resist reduces the imaging contrast

EUV thin film evaluation report

Target : Pitch=32nm, L/S=17.5nm/14.5nm

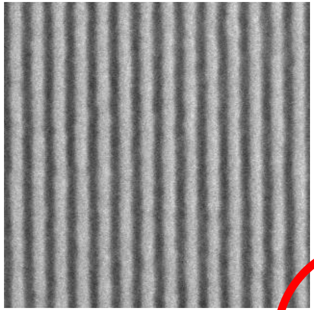
G Lorusso, et al, "Metrology of thin resist for high NA EUVL "Proc. SPIE 12053, Metrology, Inspection, and Process Control XXXVI SPIE (2022)

MOR : FT=12nm / UL1=20nm



3σ =**0.12** nm @Vacc=300V

CAR : FT=20nm / UL1=20nm



3σ =**0.13** nm @Vacc=100V

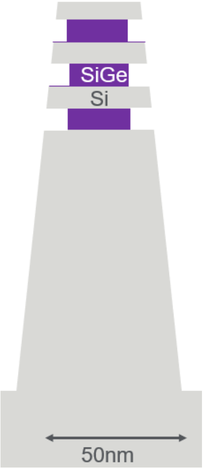
High-precision Dynamic Repeatability of MOR/CAR thin film resist wafers confirmed at low LE.

High Voltage

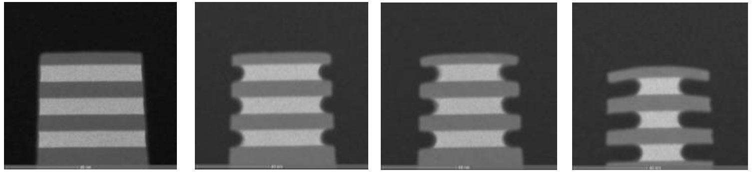
Nanosheet Recess Metrology using HV

G Santoro et al, "Recess metrology challenges for 3D device architectures in advanced technology nodes" Proc. SPIE 12053, Metrology, Inspection, and Process Control XXXVI SPIE (2022)

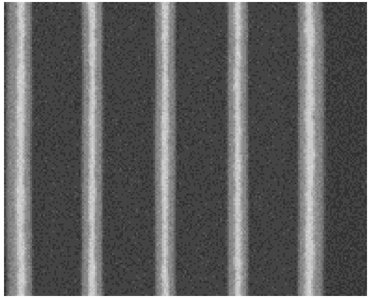
Recess Metrology



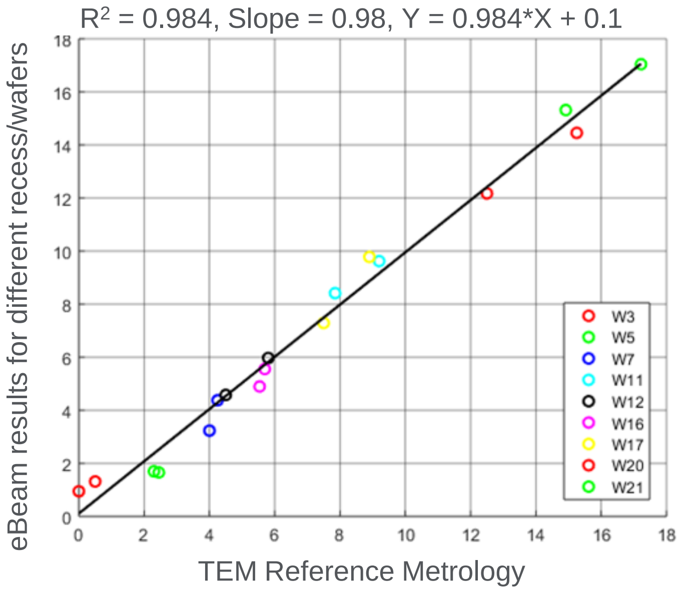
TEM



HV SEM



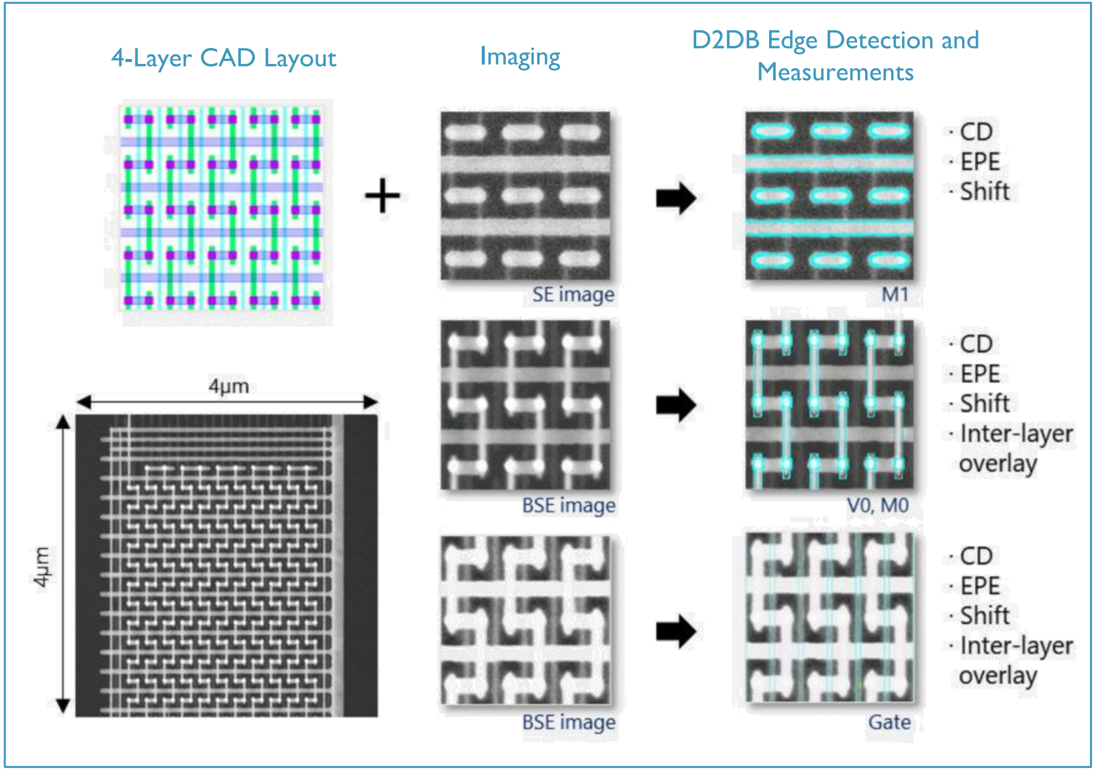
Recess Metrology Validation



High Voltage SEM recess metrology

Multilayer Metrology

S Kang et al, “Advanced high-voltage e-beam system combined with an enhanced D2DB for on-device overlay measurement” Proc. SPIE 12496, Metrology, Inspection, and Process Control XXXVII (2023)



- CD
- EPE
- Shift

- CD
- EPE
- Shift
- Inter-layer overlay

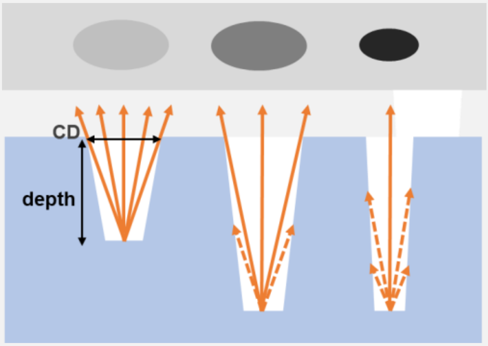
- CD
- EPE
- Shift
- Inter-layer overlay

M1, V0, M0 and Gate multilayer D2DB measurements of CD, EP, OVL, Inter-layer OVL

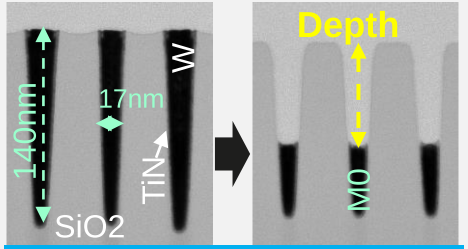
Backscattered

CFET Gray Level Metrology for Vertical EPE

W. Sun, et al., In-line metrology for vertical edge placement control of monolithic CFET using CD-SEM, Proc. SPIE. 12496, Metrology, Inspection, and Process Control for Microlithography XXXVII, (2023)

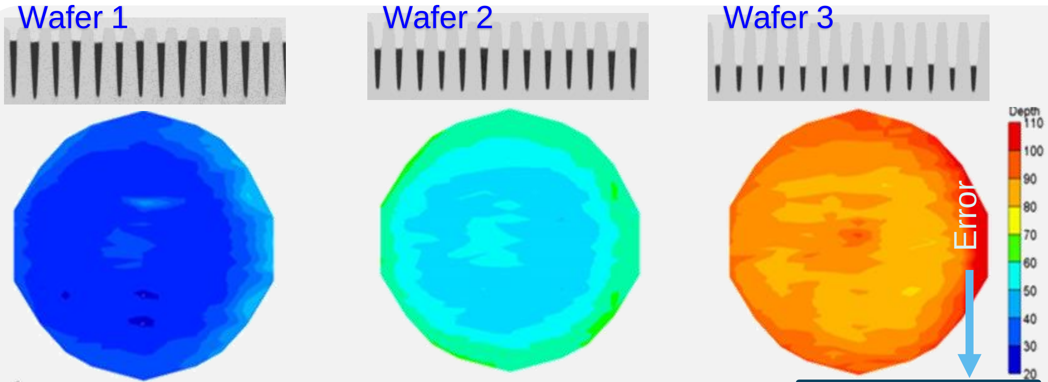


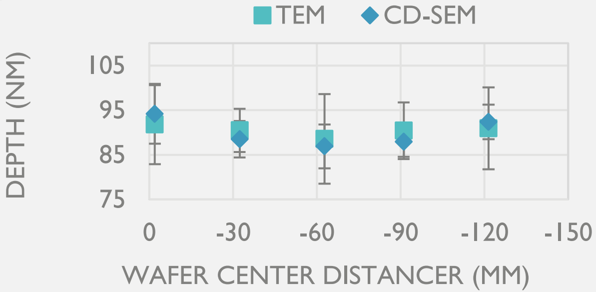
BSE intensity / CD ~ Depth

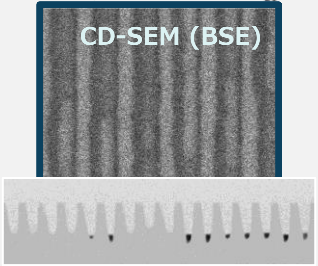


High AR W metallization and etch back

Key Process for Monolithic CFET







Good Correlation Coefficient (~0.85) with TEM X-SEC

Abnormalities can be confirmed with SEM images

Gray level metrology enabling accurate Vertical Edge Placement control

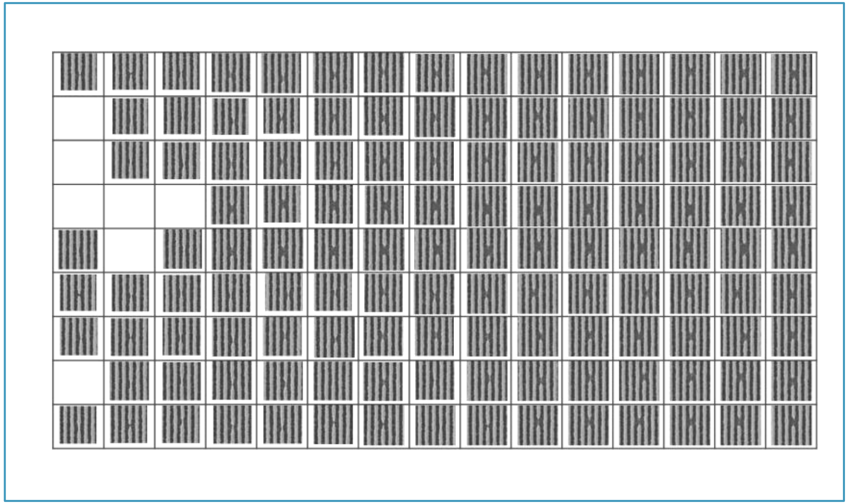
Beam current

Programmed defect matrix

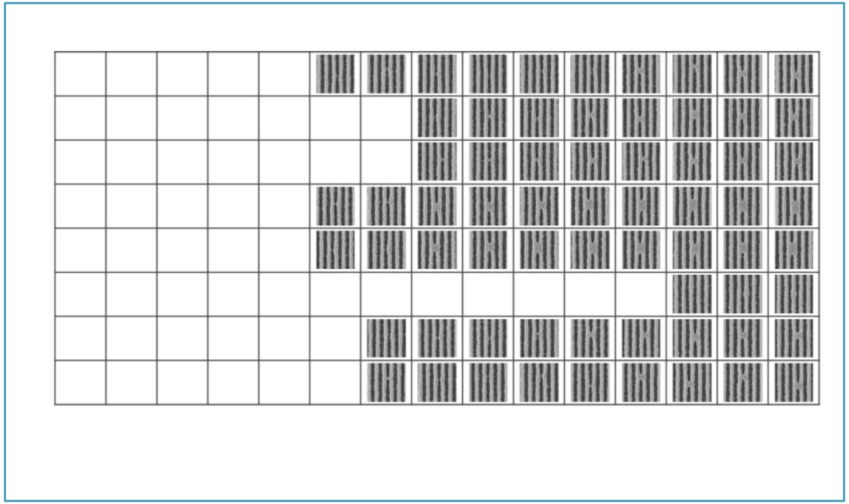
P32nm, 30nm Target FT
CG6300, Stochalis

- CD SEM was used (small FOV, small pixel size, large number of frames) to review the programmed defect matrix

Breaks



Bridges

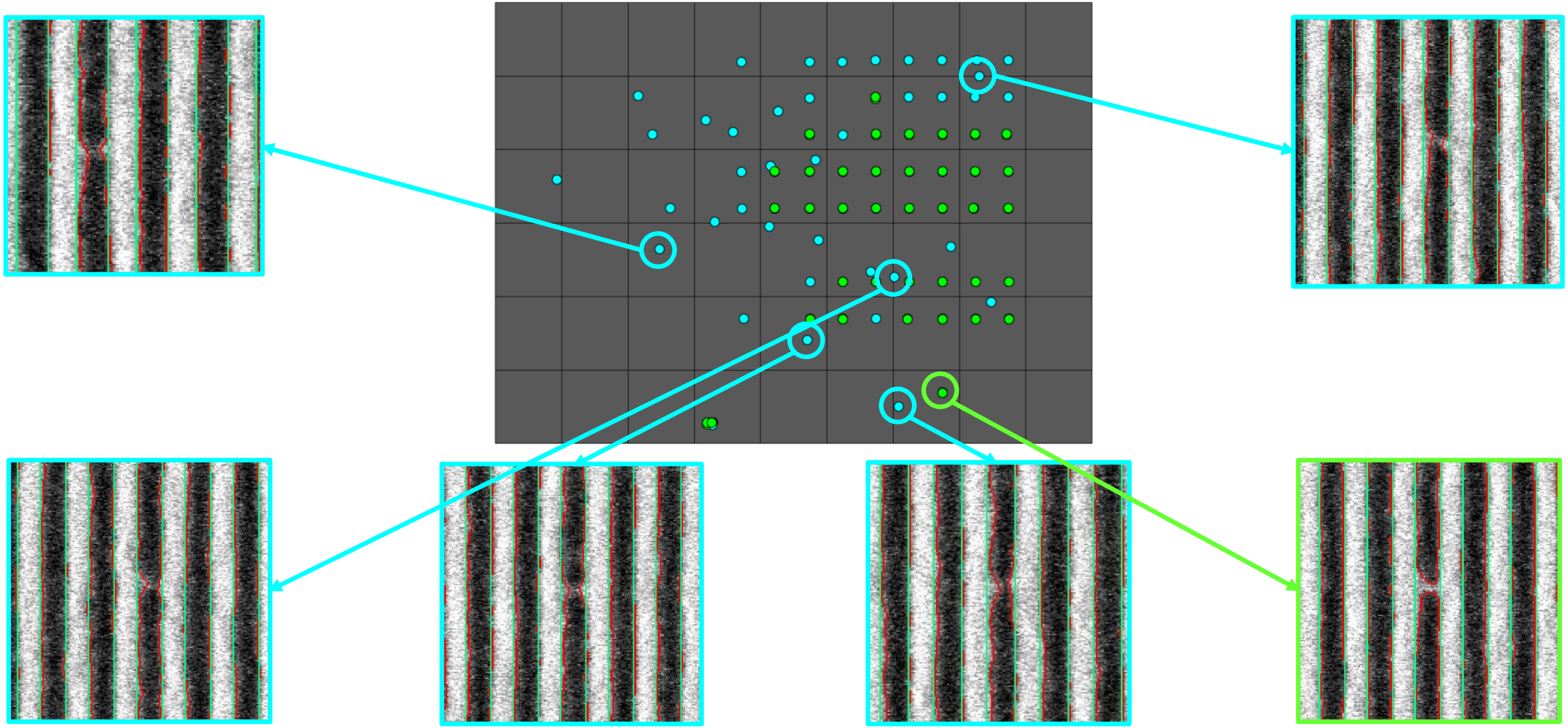


- Programmed defect matrices for breaks and bridges were used to assess printability.
- Almost all printing (both brides and brakes) defects are detected

e-beam Inspection – Random defects

🟩 Full Bridges
🟦 Protrusion

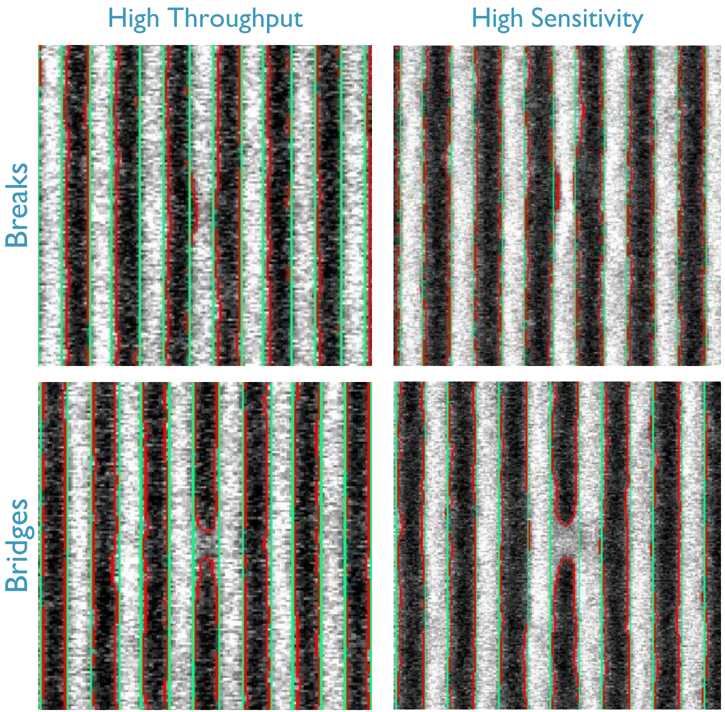
P32nm, 30nm FT, full PD matrix inspected
GS1000, MMI, area inspected 150x100µm



- E-beam inspection is able to capture very small random defect, both protrusion and necking

High Throughput mode vs High Sensitivity mode

G. Lorusso, et al., Dry Resist Metrology Readiness for High-NA EUVL, Proc. SPIE. 12496, Metrology, Inspection, and Process Control for Microlithography XXXVII, (2023)

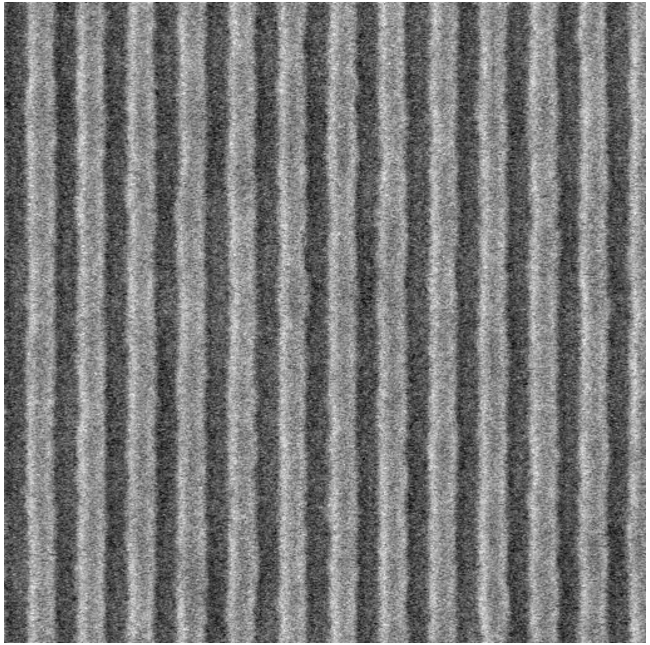


- High throughput mode improves throughput 14 x with respect to high sensitivity mode (from 105 h/mm^2 to 7.5 h/mm^2)
- Hight throughput mode decreases the sensitivity of 12% for Breaks and 24% for Bridges

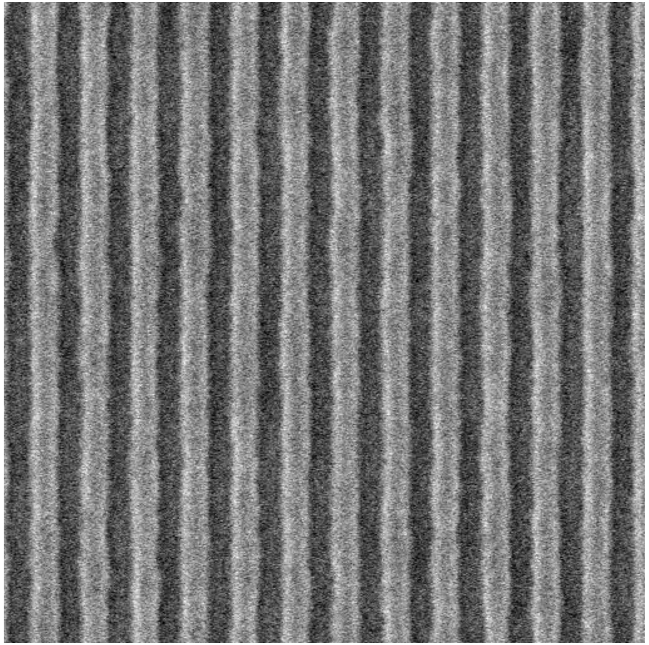
AI

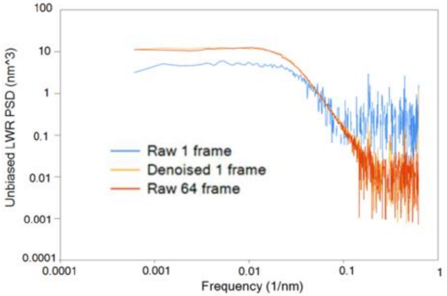
AI Denoising

Denoised 1 Frame



Raw 64 Frames





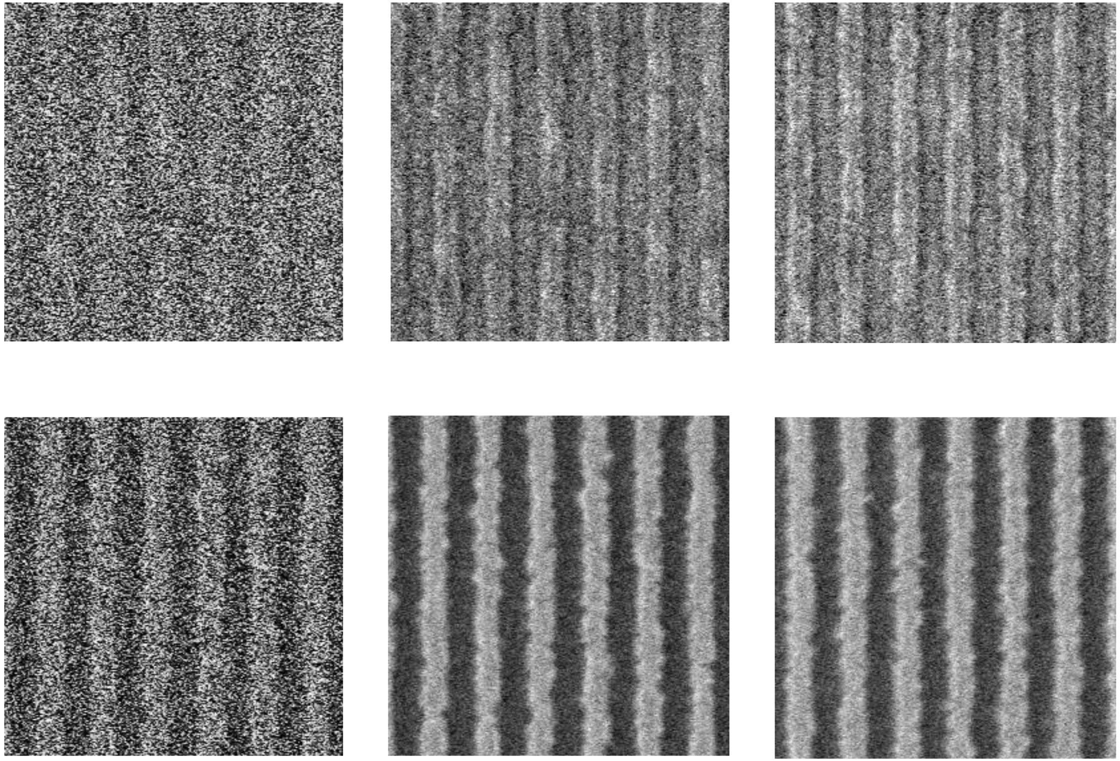
- Good PSD match between denoised images and raw 64 frame images.

AI Denoising of Thin Resist

M. Kim, et al., Frequency-informed deep-learning denoising method supporting sub-nm metrology for high NA EUV lithography,

Resist 1 15nm UL1

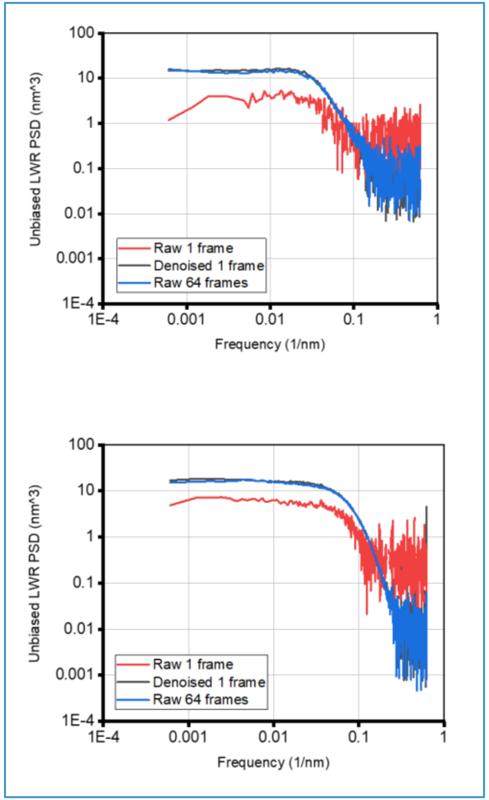
Resist 2 12nm UL2



Raw 1 Frame

Denoised 1 Frame

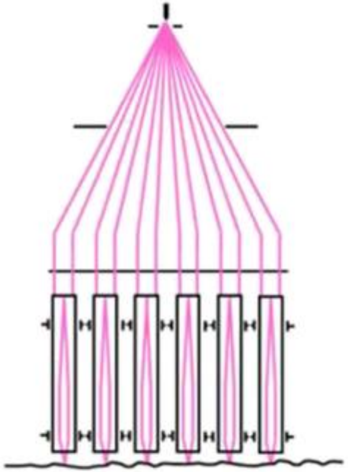
Raw 64 Frames



- Single AI model working for all process conditions with different noise levels.

Multibeam

Multi-beam Systems



MAPPER Lithography
13,200 microcolumns
5 keV

Business | April 27, 2022

ASML installs the first HMI eScan 1100 multibeam system

- Development of high-throughput multi-beam systems on its way

Conclusions

Conclusions

- The increasingly strict ICM requirements are the environmental reason that is forcing e- beam metrology to evolve fast.

- E-beam technology is taking advantages of its ability to re-define and re-use its critical parameters in a flexible way to occupy new application spaces. More specifically:

    - Low Voltage (Thin resist)
    - High Voltage (3D metrology)
    - Backscattered (Vertical EPE)
    - High Beam Current (defectivity)
    - AI (Denoising)
    - Multi-beam (Throughput)

- We expect this trend to continue to overcome the many obstacles standing in the way of Moore's law.

Acknowledgments

- We wish to thank everyone for the many useful discussions and for the support for this work.

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embracing a better life