EUV Mask technology : Ready for 5nm and beyond.

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DNP

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Introduction: Photomask Market Analysis

Confidential

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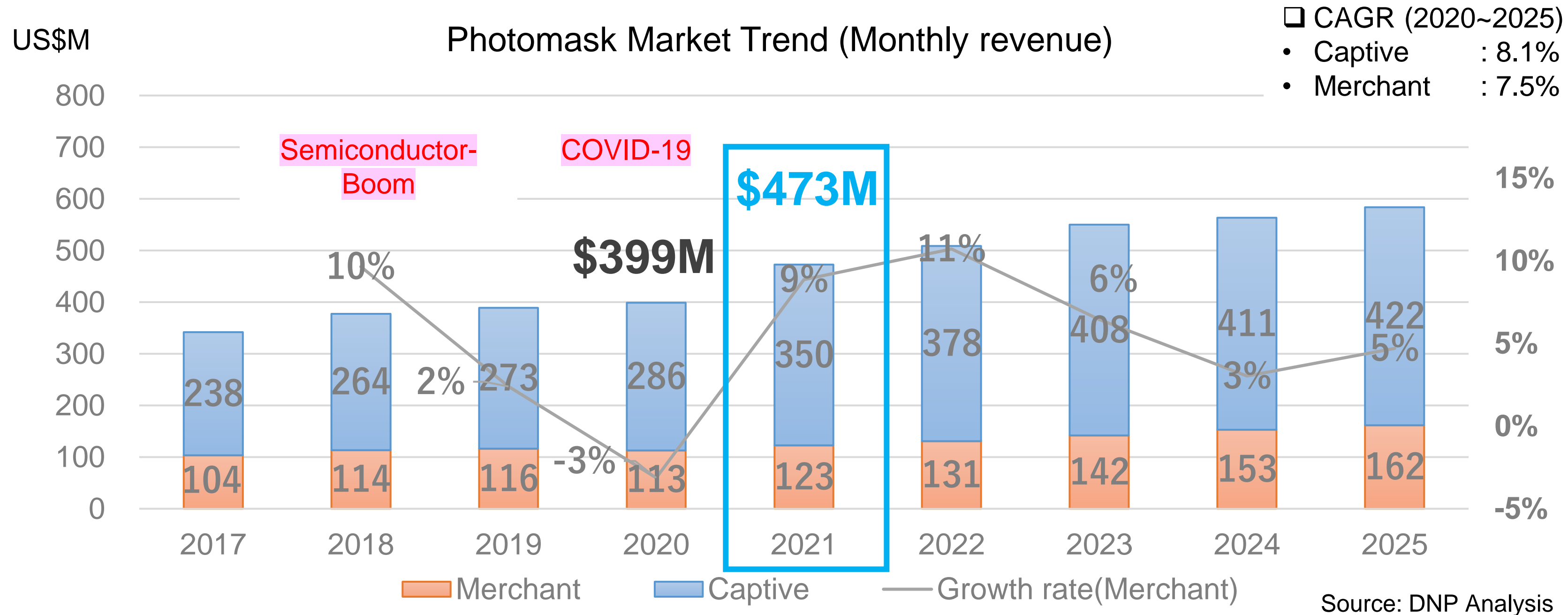

❑ CAGR (2020~2025)

- Captive : 8.1%
- Merchant : 7.5%

Source: DNP Analysis

- Y2021 Photomask market will be grown significantly by strong mask demands related to high-performance computing, smartphone, and automotive device. This trend continues until Y2022 at least.
- Y2021 Merchant market is expected to increase by 9% (YoY). Currently almost all the merchant mask suppliers have been maintained high operational rate (>90%).
- Y2021 Captive market continues to expand by 22%(YoY) due to strong needs of EUV masks for 7nm/5nm Logic devices.

Introduction: -IRDS roadmap-

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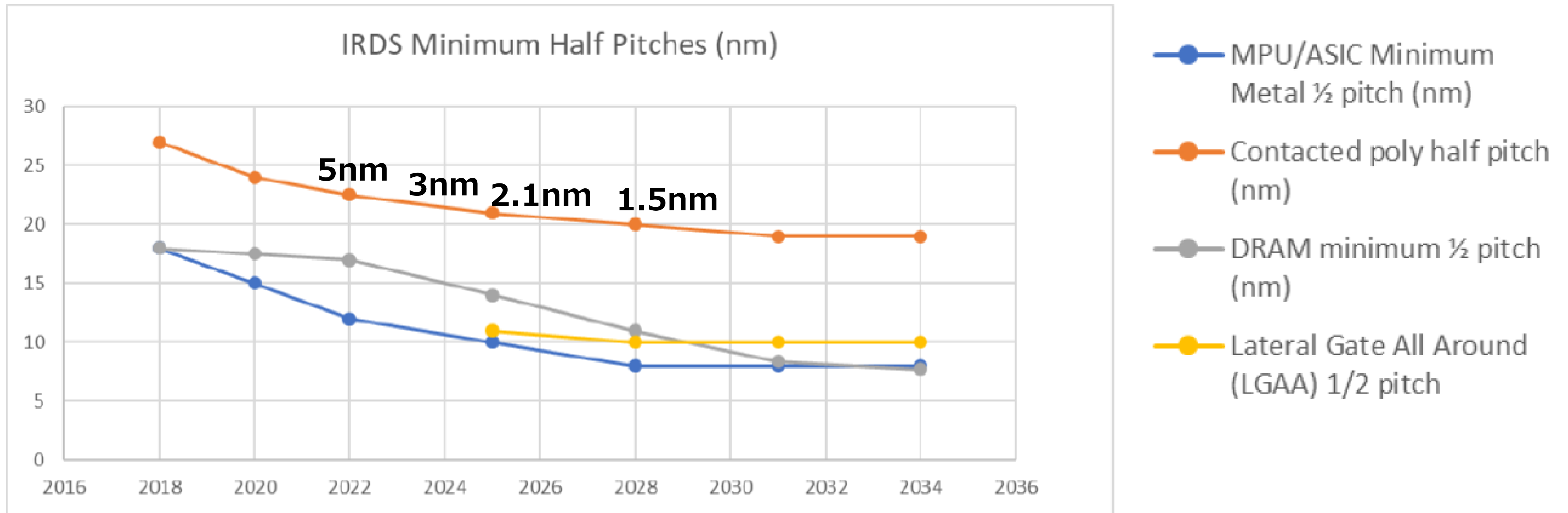
IRDS roadmap Minimum Half Pitches.

*IRDS 2020 SPIE Meeting



MPU/ASIC minimum dimension will shrink to 2028.

Introduction -IRDS roadmap-

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IRDS roadmap for Litho Requirement

*IRDS 2020 Summer Public Meeting

- **5nm node Logic is production status in 2021.**
- **Minimum feature size**
  - 15nm(MMHP=Line)
  - 15-16nm(Cont-Poly CD=Hole)
- **On mask level target size (4X)**
  - <60nm(Main L/S and hole)
  - <30nm(Assist)

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
DRAM							
DRAM minimum ½ pitch (nm)	18	17.5	17	14	11	8.4	7.7
Key DRAM Patterning Challenges	Resolution improvements at reasonable cost						
CD control (3 sigma) (nm) [B]	1.8	1.8	1.7	1.4	1.1	0.84	0.8
Minimum contact/via after etch (nm) [H]	18	17.5	17	14.0	11	8.4	7.7
Minimum contact/via pitch(nm)[H]	54	53	51	42	33	25.2	23
Overlay (3 sigma) (nm) [A]	3.6	3.5	3.4	2.8	2.2	1.68	1.5
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
Key MPU/Logic Patterning Challenges	EPE, Single Exposure for <36nm pitch, Cost of EUV patterning						
MPU/ASIC Minimum Metal ½ pitch (nm)	18	15	12	10	8	8	8
Metal LWR (nm) [C]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Metal CD control (3 sigma) (nm) [B]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Contacted poly half pitch (nm)	27.0	24.0	22.5	21.0	20.0	19.0	19.0
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Gate LER (nm) [C]	0.8	0.7	0.6	0.5	0.4	0.4	0.4
Gate CD control (3 sigma) (nm) [B]	1.1	1.0	0.9	0.7	0.6	0.6	0.6
Overlay (3 sigma) (nm) [A]	3.6	3.0	2.4	2.0	1.6	1.6	1.6
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0	12.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
Fin CD control (3 sigma) (nm) [B]	0.80	0.70	0.60				
FIN LER (nm) [C]	0.80	0.49	0.42				
Lateral Gate All Around (LGAA) 1/2 pitch				11	10	10	10
LGAA minimum width				7	6	6	6
LGAA CD control (3 sigma) (nm) [B]				0.7	0.6	0.6	0.6
GAA LER (nm) [C]				0.49	0.42	0.42	0.42
MPU/ASIC minimum contact hole or via pitch (nm)	51	42	34	28	23	23	23
Via CD after etch (nm) [H]	18	15	12	10.0	8.0	8.0	8.0
Contact CD (nm)after etch - finFET, LGAA	18	16	17	18	20	18	18

MBMW principle

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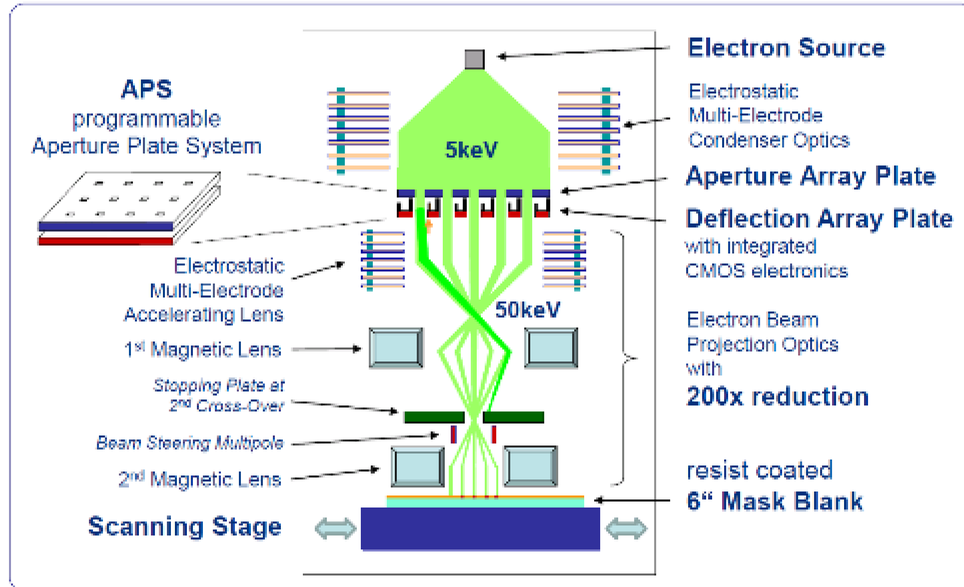
Principle : Multi-Beam with raster scan



DNP tool

Characteristics / Advantages

- **Multi-Beam : 262,144 beams**
- **120G Data Path**
- **High current density of E-beam source and Raster scan system.**

➔fixed writing time of around 12hrs/plate

- **High Accuracy on CD : Quad-grid and 16 Gray beam**
- **High Accuracy on IP : Air bearing stage system**

DNP installed MBMW 2017 and release production 2018.

MBMW principle -difference b/w VSB and MBMW-

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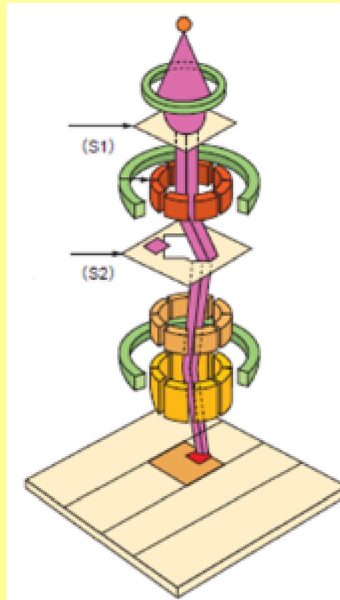
VSB=Vector Scan Beam | **MBMW=Multi Beam Mask Writer**

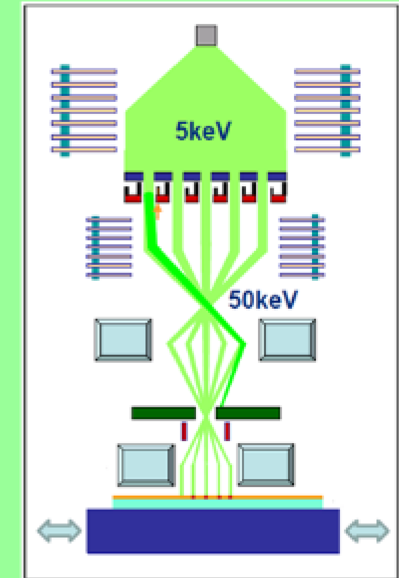
VSB

- Variable Shaped Beam mask writer
- One shaped vector beam
- Writing time dependency
  #shot counts
  #resist sensitivity



MBMW

- Multi Fixed Beam Mask Writer
- 262-thousand raster beams
- Writing time independency for pattern complexity
- Designed for mid and low sensitivity resist



MBMW technology is necessary for high end mask manufacture.

Writing time comparison

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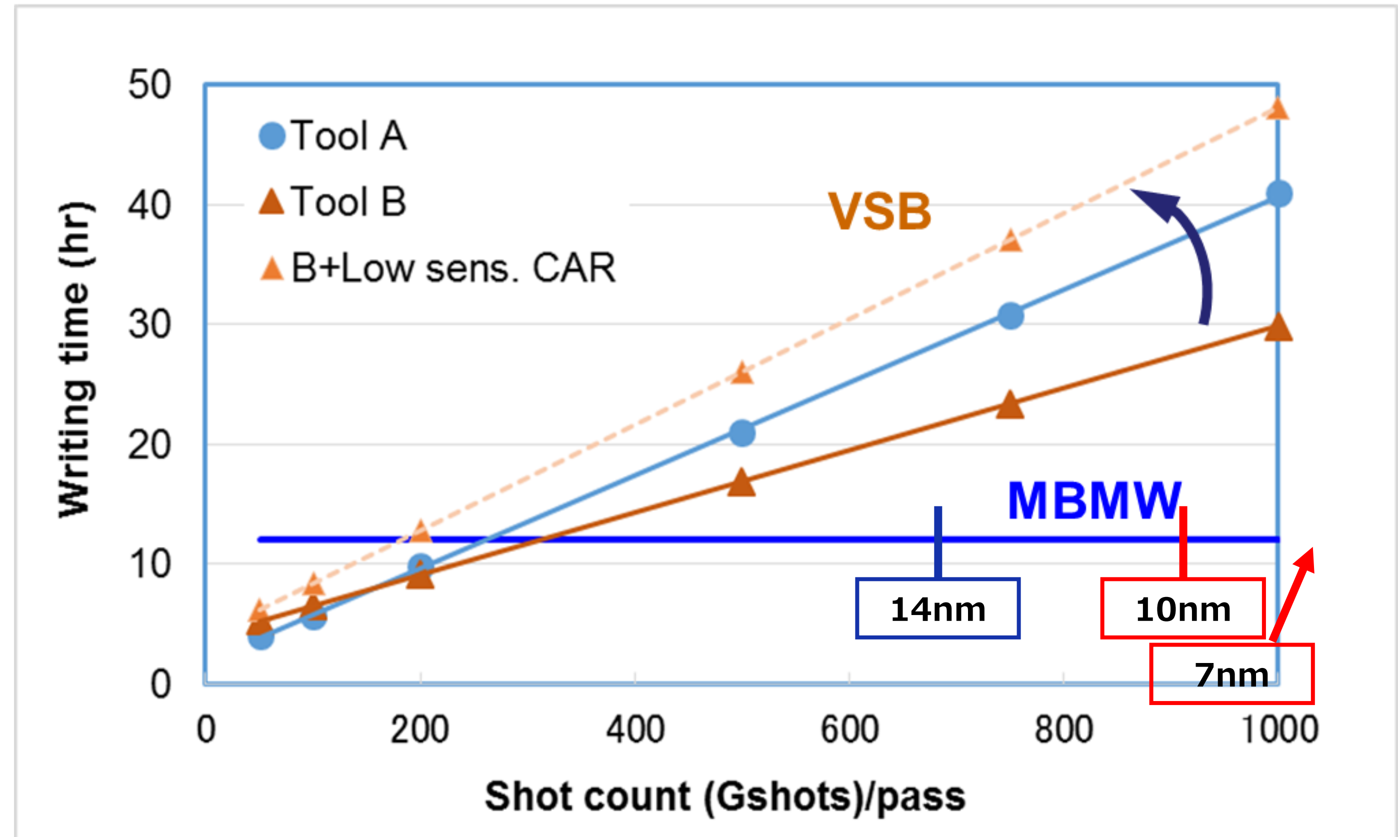
- High-End mask need for over 700 Gshots for VSB.
- MBMW using raster scan system, no impact shot count.(depends on writing area)
- Shorter writing time can enable the use of lower sensitivity resist, which enables significant improvements in resolution.



MBMW technology is good productivity!

Technology Trends -5nm EUV mask structure and Resolution-

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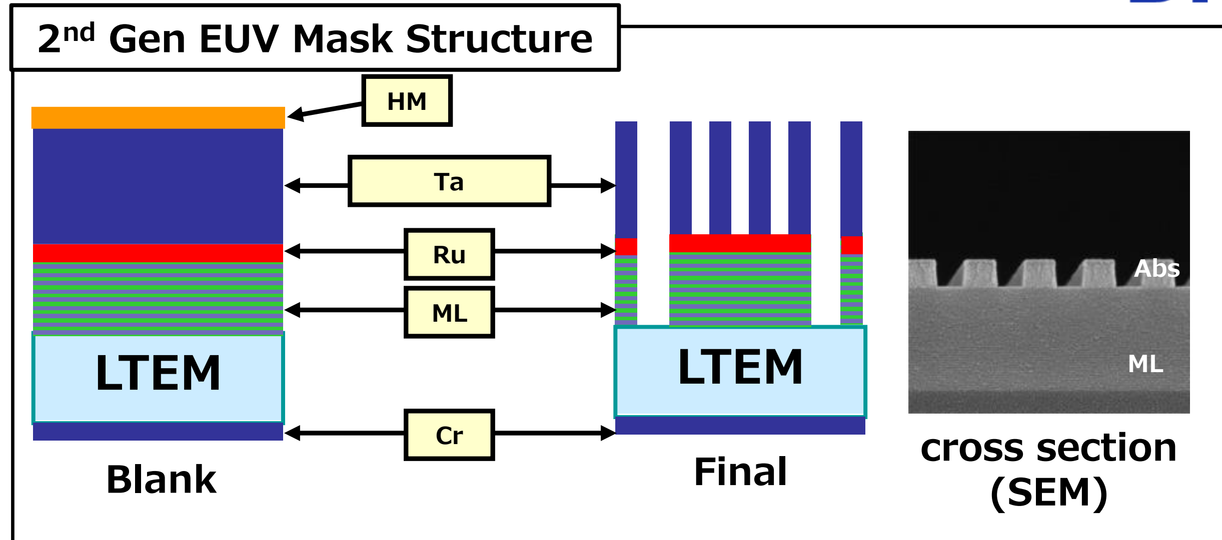
- DNP established 2nd gen EUV process, it using HM technology and thinner Low sensitivity PCAR resist.
- Absorb layer is 60nm it can be better printability.
- EUV mask can achieve under 30nm for L/S pattern also to use Low-sensitive P-CAR process, for Hole pattern can be formed under 40nm stable.



EUV P-CAR	Isolated Space	Line & Space	Isolated Line	Dense Hole	Isolated Hole
minimum resolution	18nm	26nm	34nm	30nm	36nm
60nm					

Position Accuracy

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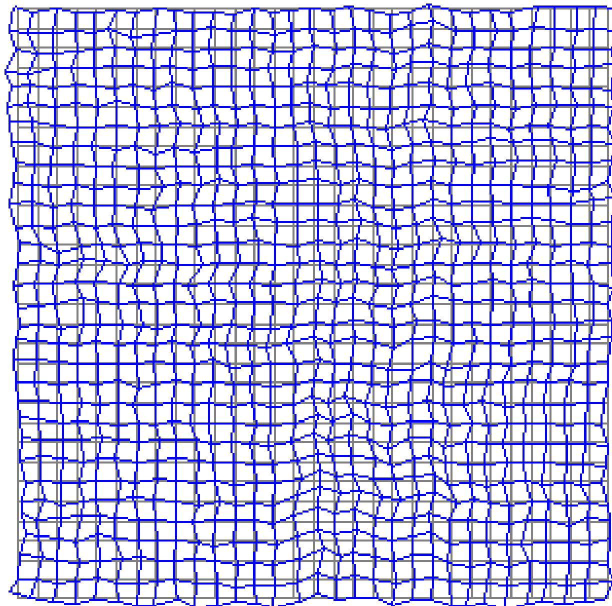
- Position Accuracy performance of MBMW Low-PCAR EUV process.

Target spec:1.5nm

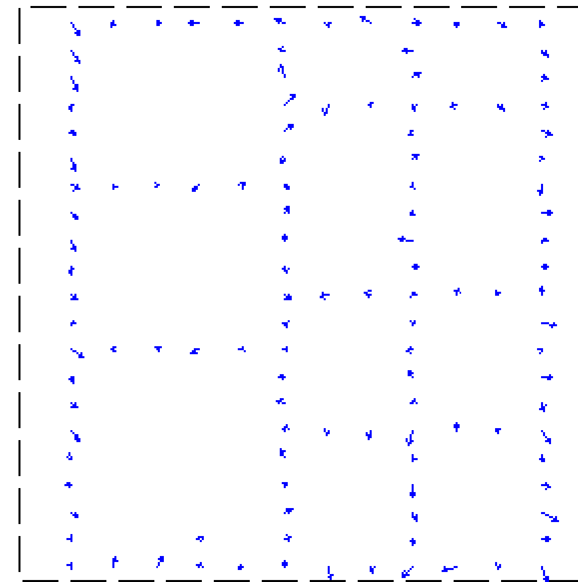
140mmx140mm cross pattern



3 sigma : 0.9/ 0.81 (X/Y)

Test mask reg map
(tool check pattern)

100mmx135mm Device mask



3 sigma : 1.35 / 1.21 (X/Y)

Production mask reg map

MBMW Low-PCAR EUV process can achieve 1.5nm position accuracy.

Global CDU

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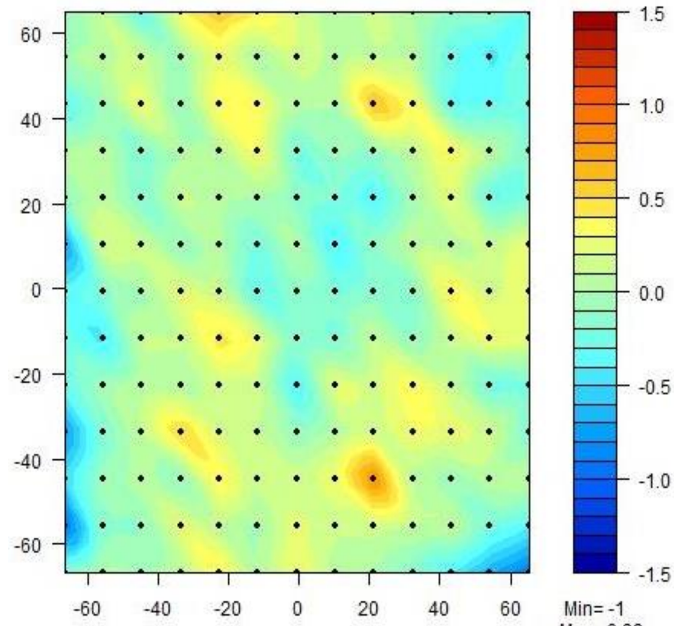
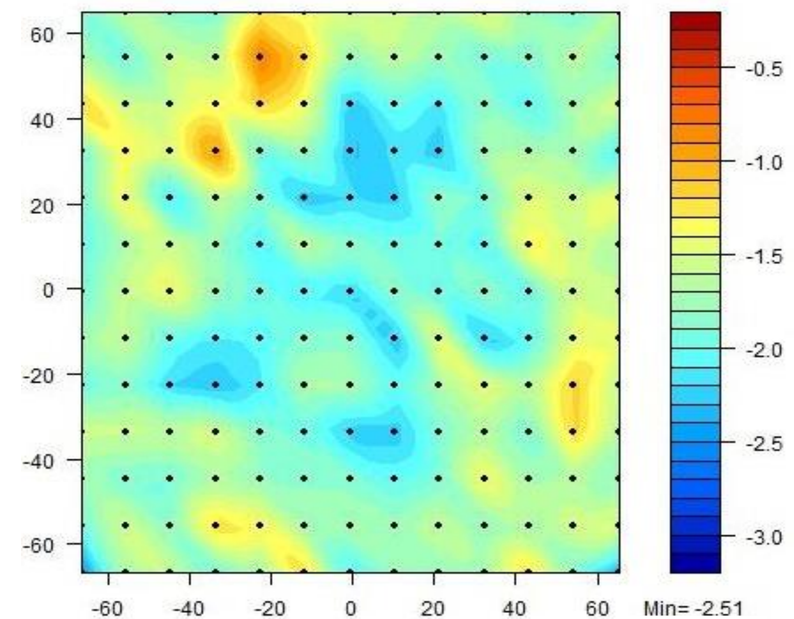
- CDU performance of MBMW Low-PCAR EUV process.

Main feature [60nm]



0.84nm[3sigma]

Assist bar [30nm]



0.93nm[3sigma]

MBMW Low-PCAR EUV process can achieve CDU performance <1.0nm main and assist feature.

LER performance

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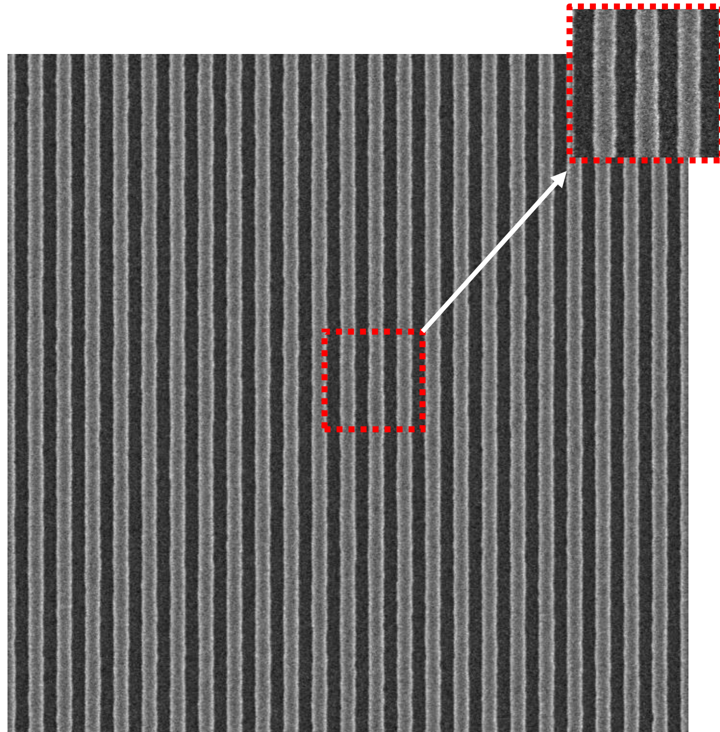
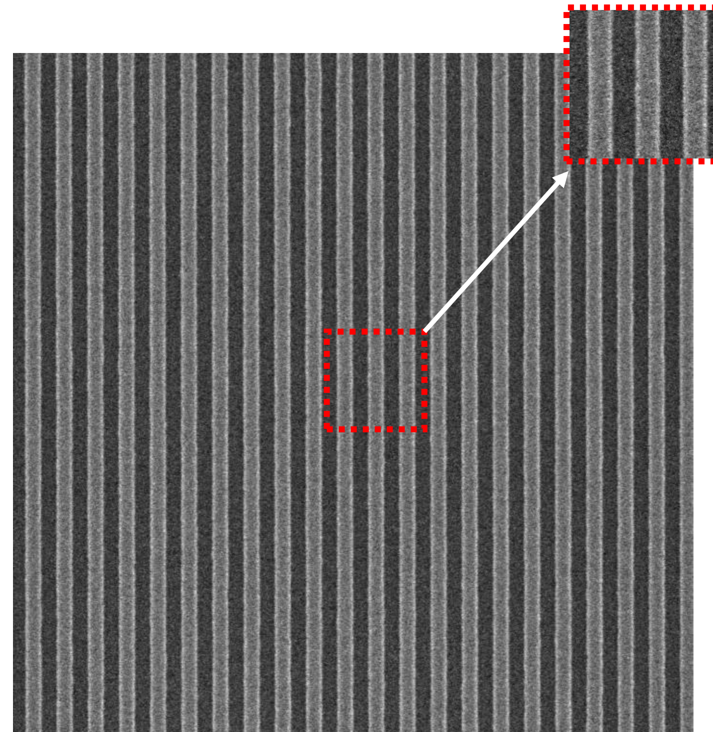
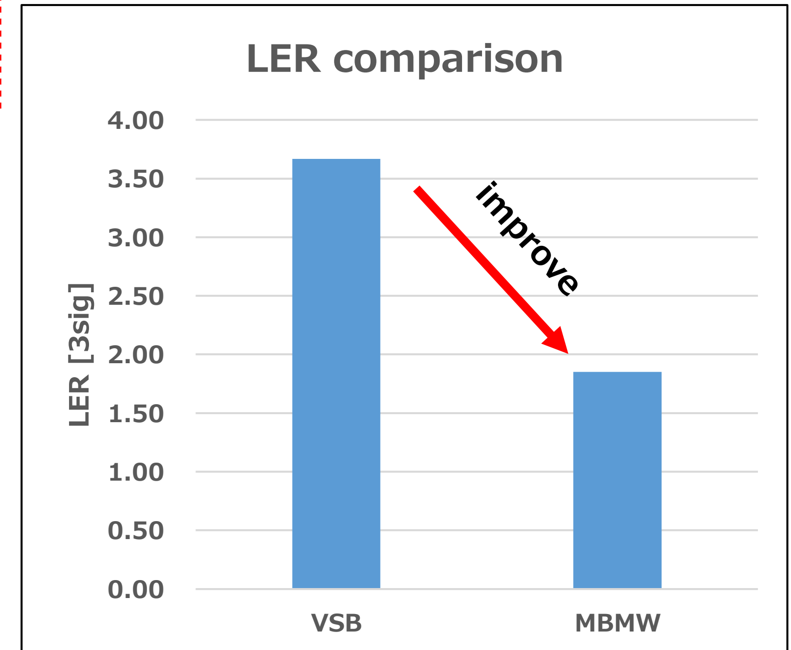
LER comparison b/w VSB PCAR and MBMW Low-PCAR.
Design:60nm Line and space


Normal PCAR


MBMW Low-PCAR



LER results

MBMW Low-PCAR EUV process can improve LER.

Local CDU analysis

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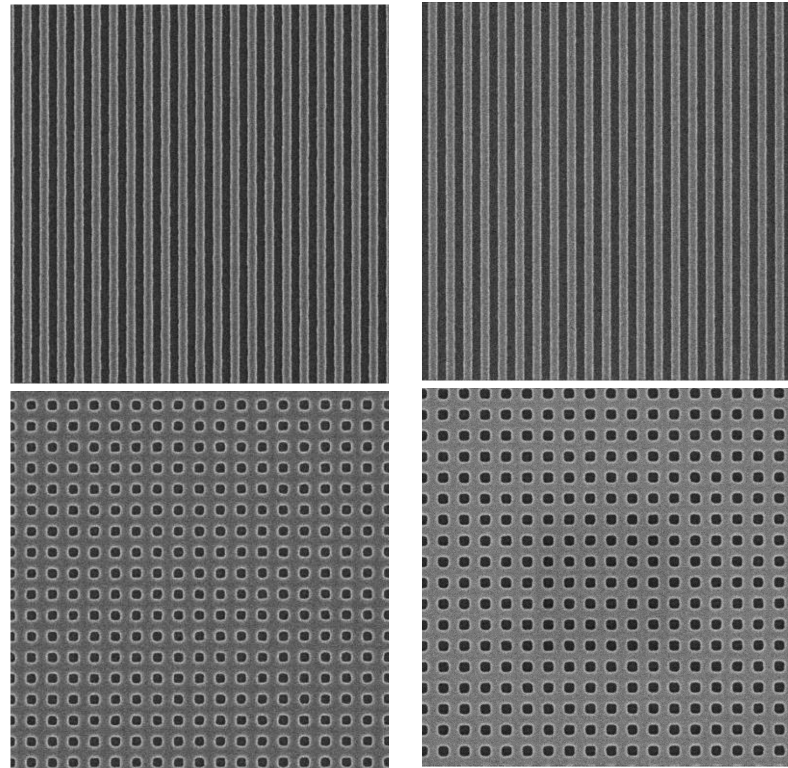
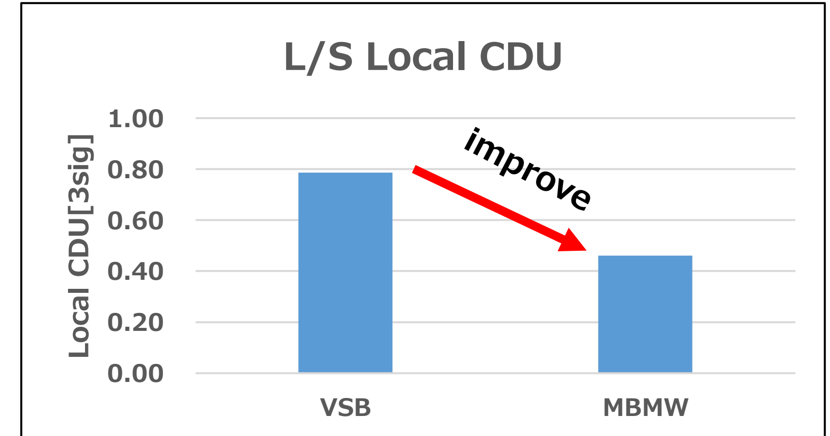
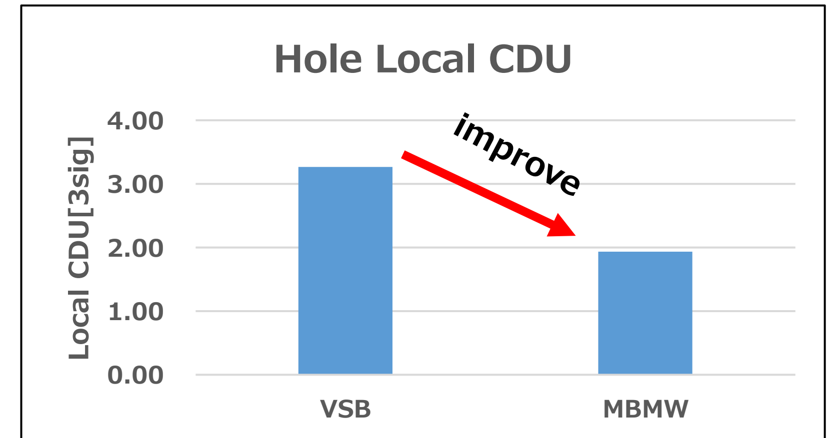
LER comparison b/w VSB PCAR and MBMW Low-PCAR.
Design:60nm L/S, 60nm Hole

- **MBMW Low-PCAR EUV process can get pattern fidelity stable, The LCDU value is improve >40% than VSB PCAR process.**
- **Low sensitive resist capability is enough for 5nm EUV technology.**



VSB PCAR **MBMW Low- PCAR**





LCDU results

Curvilinear capability

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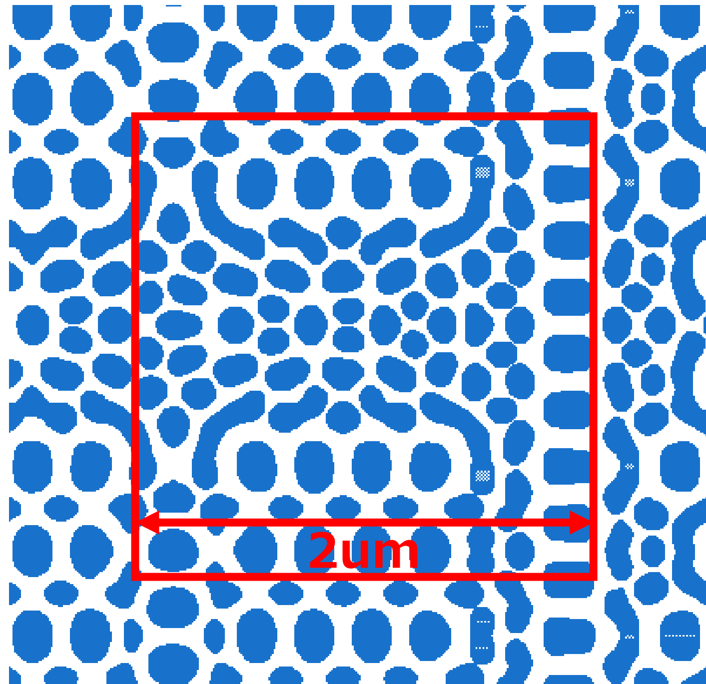
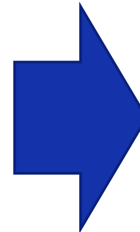
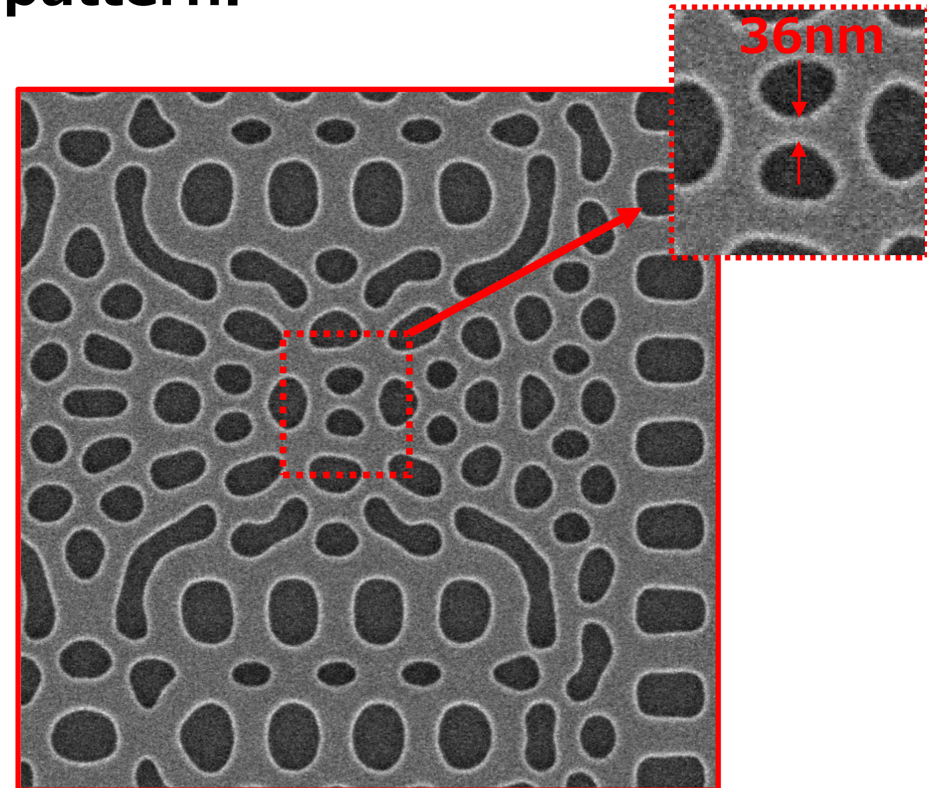
Patterning capability for curvilinear pattern.



OASIS





SEM

DNP is ready for curvilinear patterns based on MBMW Technology.
But angled pattern measurement for curvilinear has many challenge for mask technology.

Remaining challenges

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- How to measure smaller and angled pattern?
  - Measurement standards?
  - Need for Methodology study.
  - How to guarantee disposition?
- How to Guarantee the printing defects?
  - Actinic inspection tool with pellicle?
  - Need for any other inspection method e.g., EB, DUV or other?
  - EUV-AIMS or other disposition method?
- How to solve the cost issues?
- TOOL, Material supplier and EDA companies R&D work is an indispensable to solve EUV technology challenges.

Conclusion

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- For EUV mask trend that performances listed, and DNP has been achieved to drive MBMW technology.

Item	Result
Image Placement Error	0.9/0.88（X/Y）
Global CD uniformity	0.84/0.93(60nm/30nm)
Resolution （L&S/Hole）	26nm/30nm

- About EUV mask technology has many challenges, especially stochastics impact, Metrology, Productivity and cost.
- TOOL, Material supplier and EDA companies R&D work is an indispensable to solve EUV technology challenges.
- DNP supports many companies with mask technology to solve EUV technology challenges.

Thank you for your attention.