Fundamental Studies of EUV Lithography Including Shortening Wavelength at NewSUBARU Synchrotron Light Facility (Keynote)

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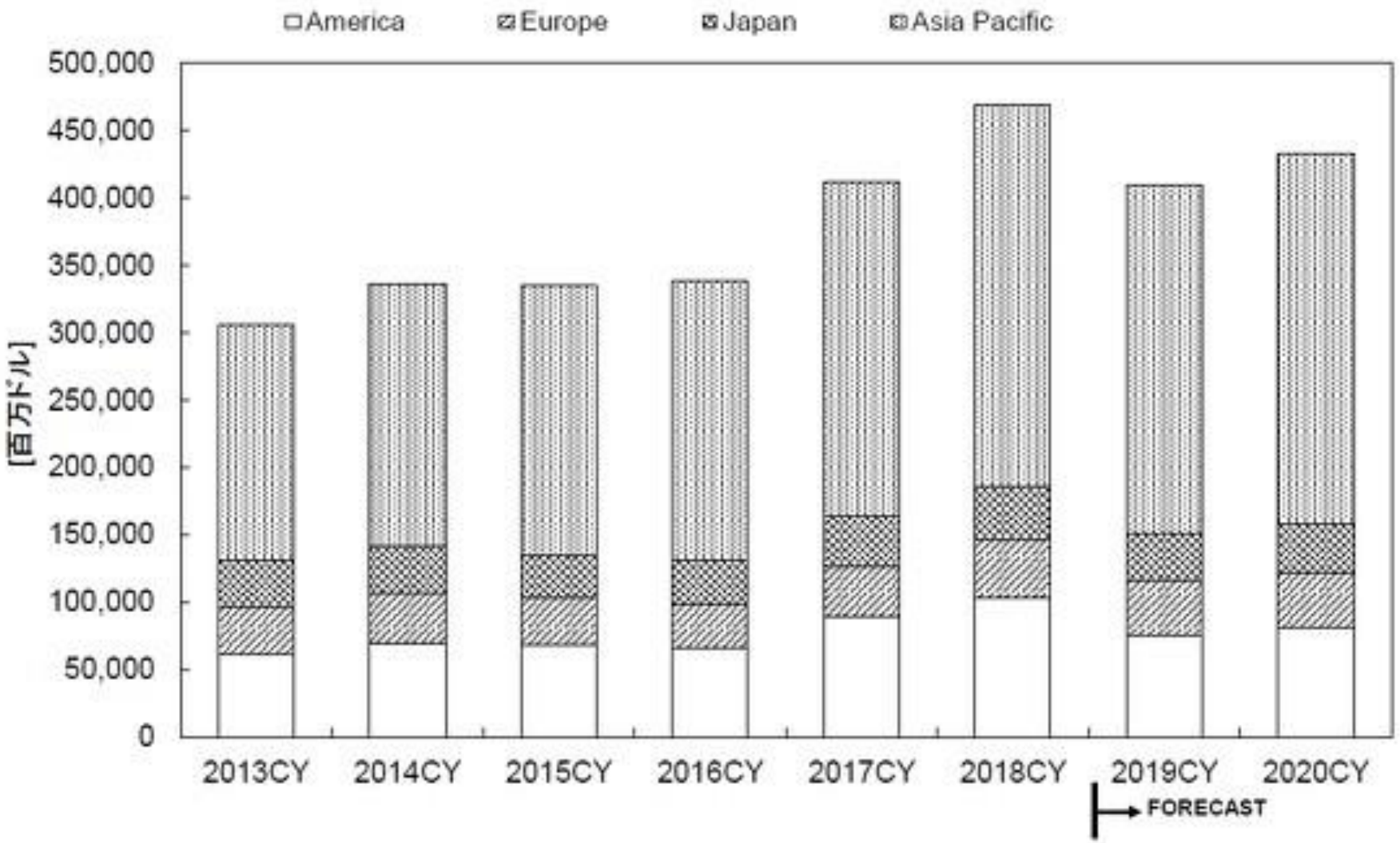
Outline

1. Introduction of “Center for EUVL”.
2. World semiconductor market and necessity of the advanced lithography
3. Overview of Tools for EUV Resist and Mask evaluations
4. Requirement of shortening the EUV wavelength
5. NS Linac as an injector of NewSUBARU
6. Summary

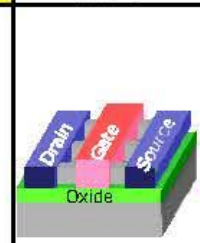
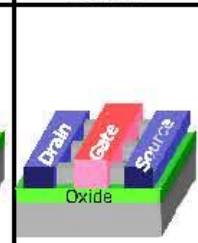
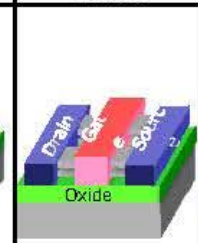
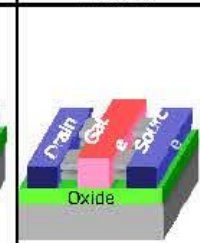
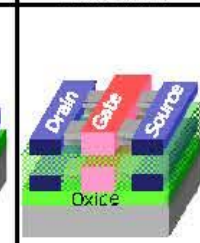
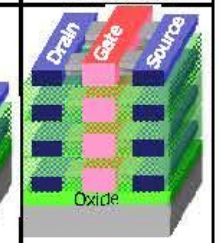
WSTS（World Semiconductor Trade Statistics）

It reached approximately 433B$ in 2020 and 5.9% increasing that in 2019.



IRDS 2020 Device, PPA, and Ground Rules Roadmap for Logic Devices

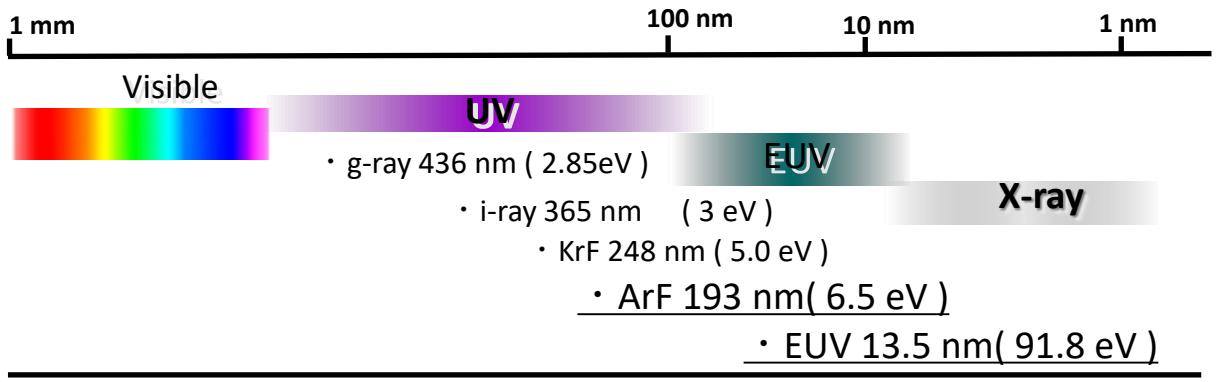
INDEX *Table MM01 - More Moore - Logic Core Device Technology Roadmap*

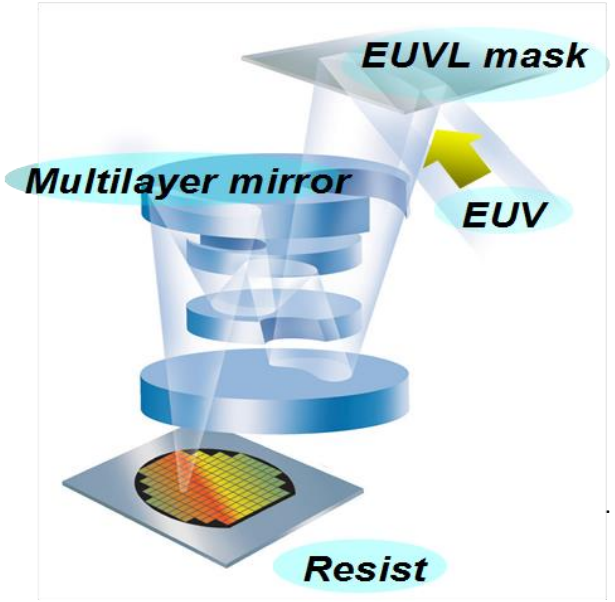
YEAR OF PRODUCTION	2020	2022	2025	2028	2031	2034
	G48M36	G45M24	G42M20	G40M16	G38M16T2	G38M16T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Mainstream device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
						
Vdd (V)	0.70	0.70	0.65	0.65	0.60	0.60
Gate length (nm)	18	16	14	12	12	12
Number of stacked tiers	1	1	1	1	2	4
Number of stacked devices	1	1	3	3	4	4
Digital block area scaling - node-to-node	-	0.75	0.78	0.79	0.52	0.50
Cell height limitation - HD	M0	M0	M0	M0	M0	M0
SoC area scalling (stacked) - node-to-node	-	0.78	0.82	0.83	0.56	0.59
CPU frequency (GHz)	3.13	3.27	3.51	3.47	3.25	2.93
Frequency scaling - node-to-node	-	0.04	0.08	-0.01	-0.07	-0.10
CPU frequency at constant power density (GHz)	3.13	2.58	2.92	2.19	1.29	0.78
Power at iso frequency - node-to-node	-	-0.08	-0.26	-0.05	-0.07	-0.09
Power density - relative	1.00	1.27	1.20	1.58	2.52	3.73
LOGIC TECHNOLOGY ANCHORS						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to mainstream CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process technology inflection	Conformal Doping, Contact	Channel, RMG	Lateral/AtomicEtch	Non-Cu Mx	3DVLSI	3DVLSI
Stacking generation inflection	2D	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D-stacking, 3DVLSI: Mem-on-Logic with Interconnect	3D-stacking, 3DVLSI: Logic-on-Logic

Lithography Trend and EUV Lithography

Rayleigh equation

$$R = k_1 \frac{\lambda}{NA}$$



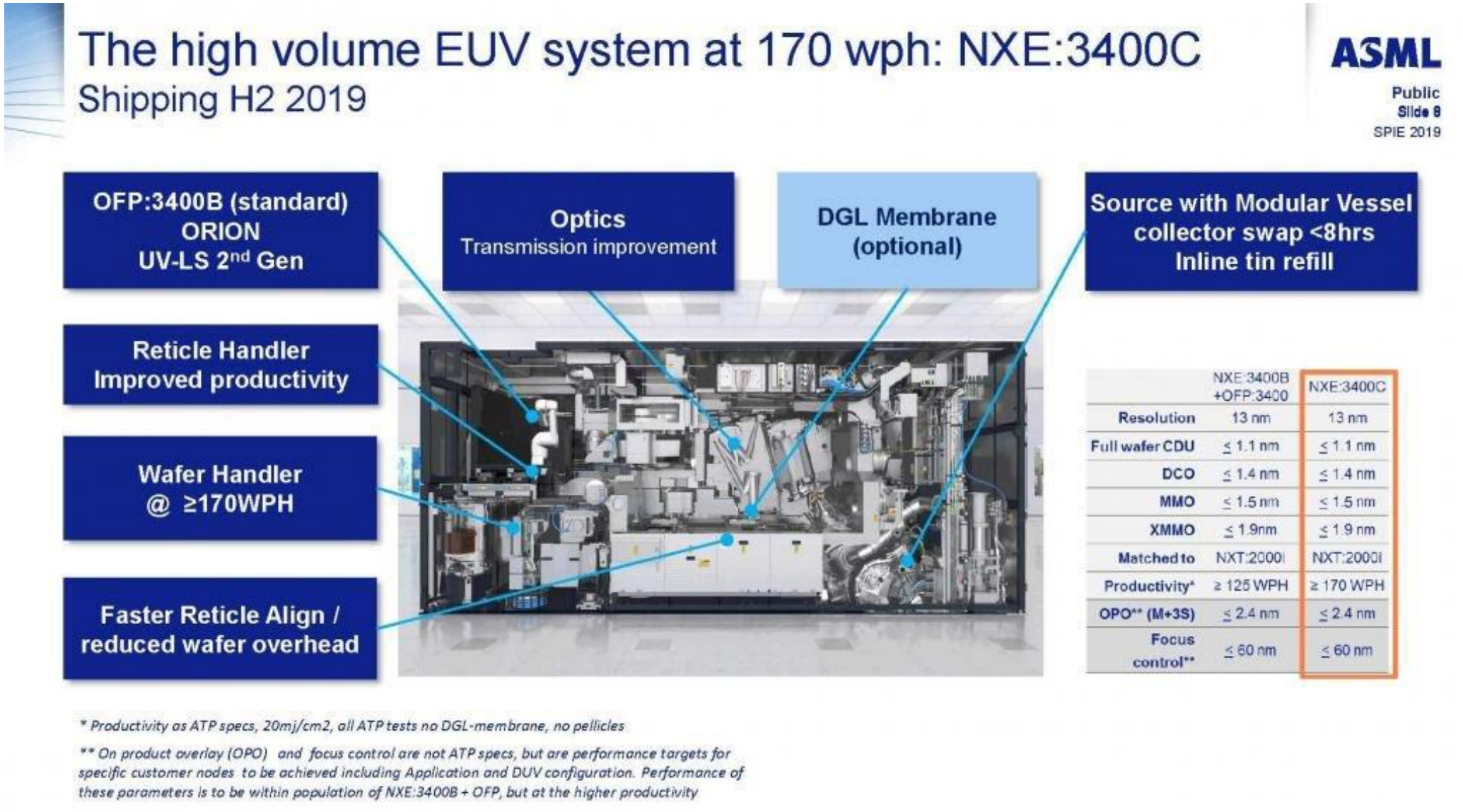


Multiple exposure of ArF immersion is a complicated technique and is not worth the cost .

Single layer resist process is effective.

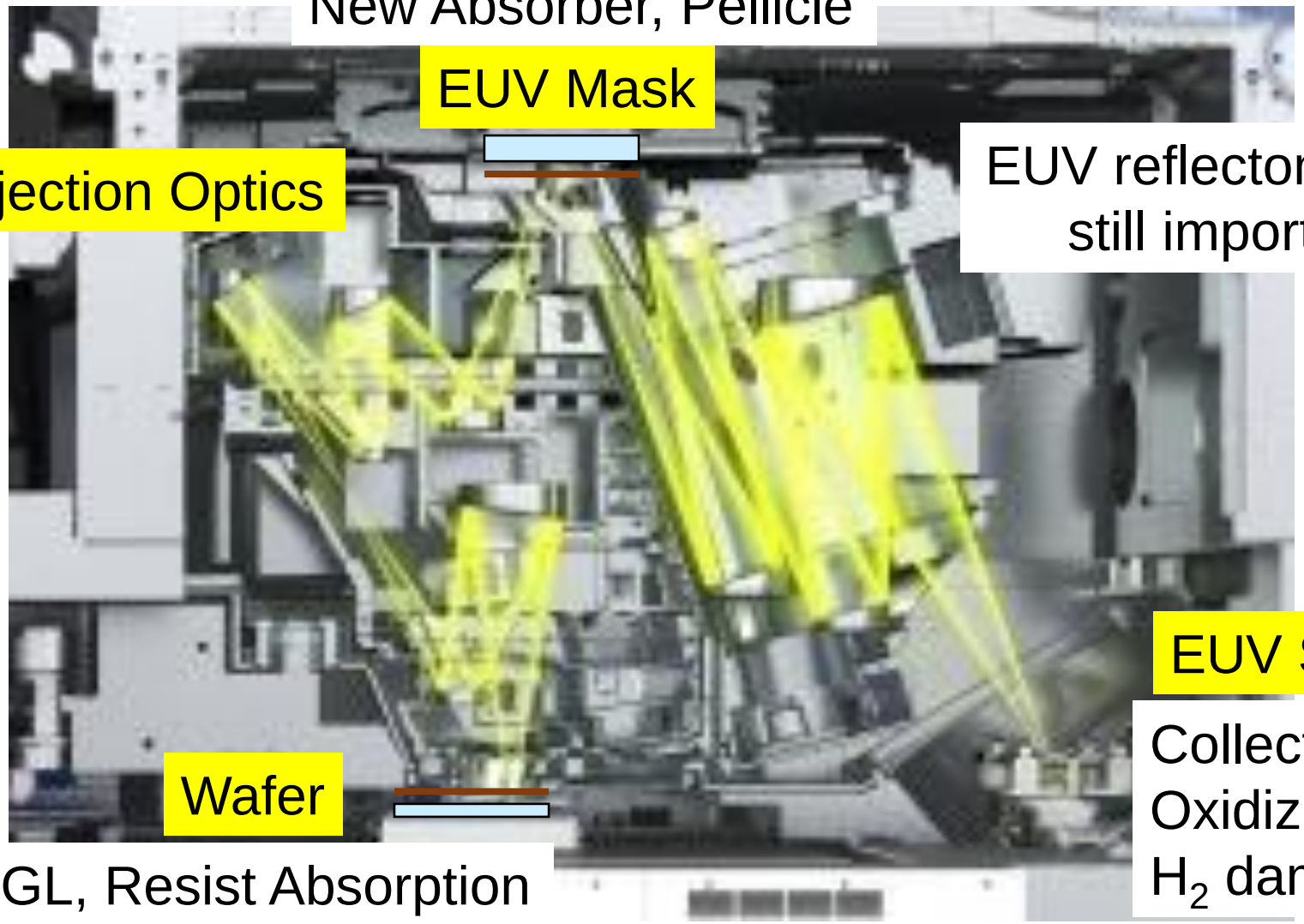
EUVL is essential for the manufacture of logic devices.

- **31 units of ASML's state-of-the-art EUV scanner "NXE: 3400 series" shipped in 2020**
- **40 units will be shipped in 2021**



Overview of EUV Exposure Tool

New Absorber, Pellicle



Reflection optics in the HVM EUV exposure tool

Necessity of the Advanced Lithography

- Improvement of integration

  Terabyte → petabyte (human brain)

- Low power consumption

  DC 3.3 V To DC 0.3 V or less

- Speed up processing

  More than 1000 times

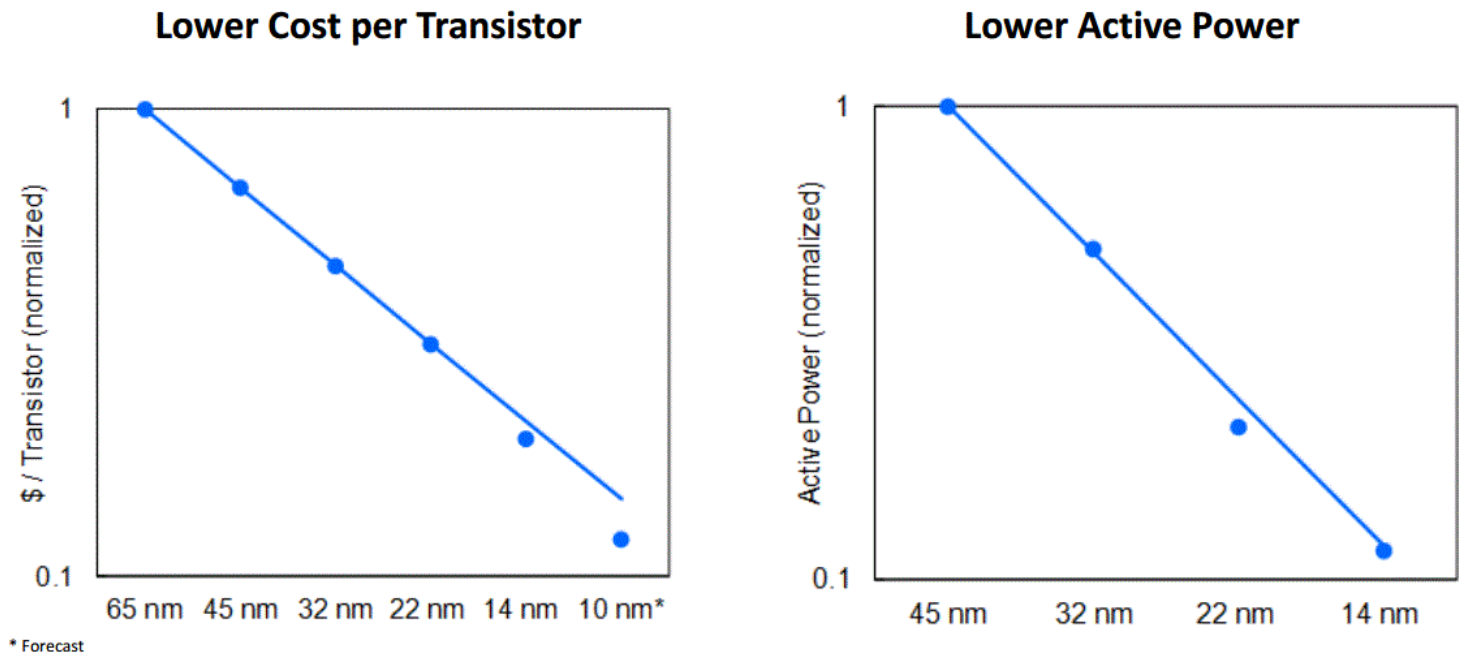
- Reduction of manufacturing cost

  1/100 to 1/1000 every 5 years

Moore's Law: Benefit for Economics and Power

Advanced lithography leads reduction of production cost and power consumption of semiconductor devices.

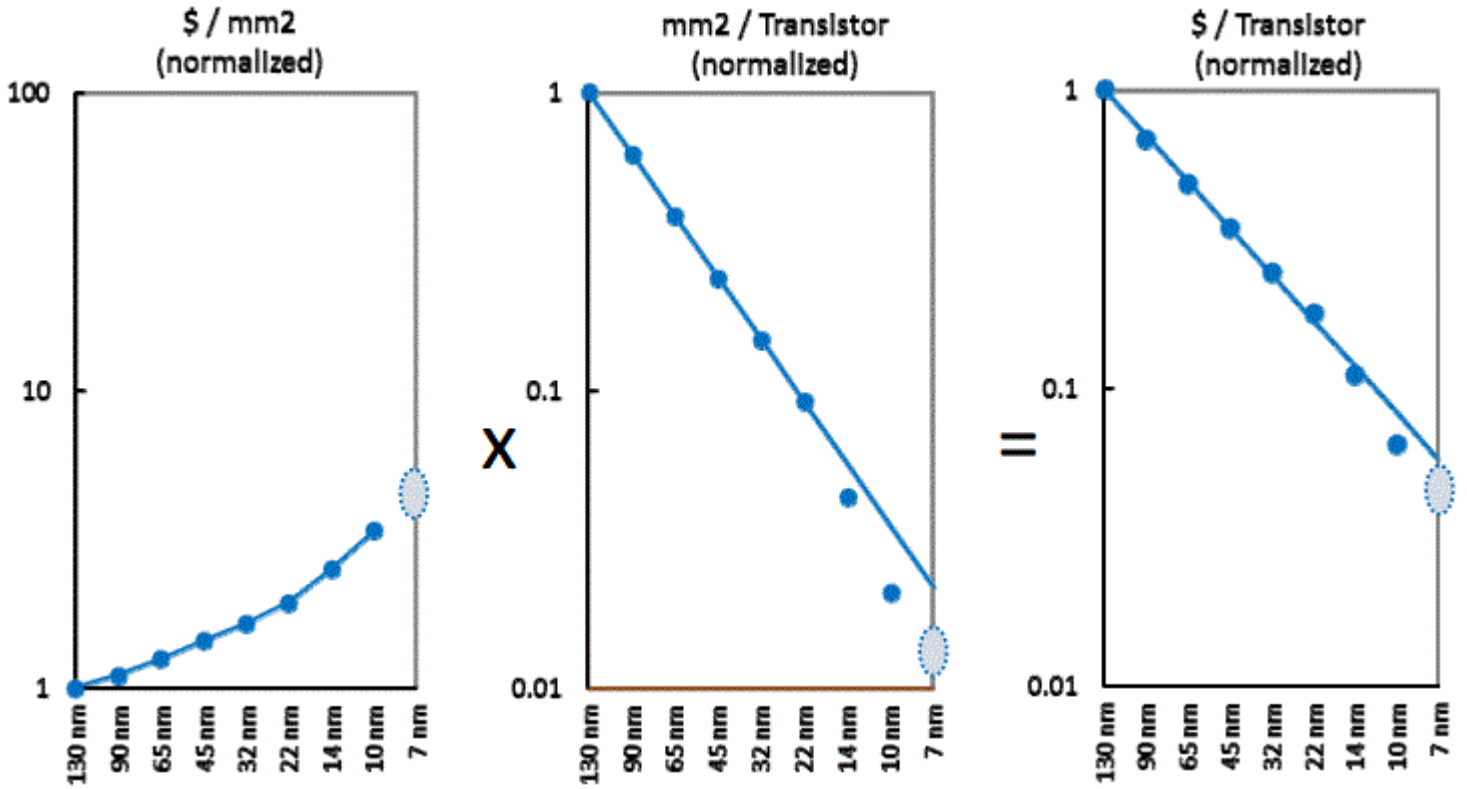
Cost and Power



Reference: Intel, Bill Holt, ISSCC 2016

Embedded Systems and Innovation Technologies for IoT Applications, Ali Keshavarzi. IEDM 2016.

Cost per Transistor ($/Tr)

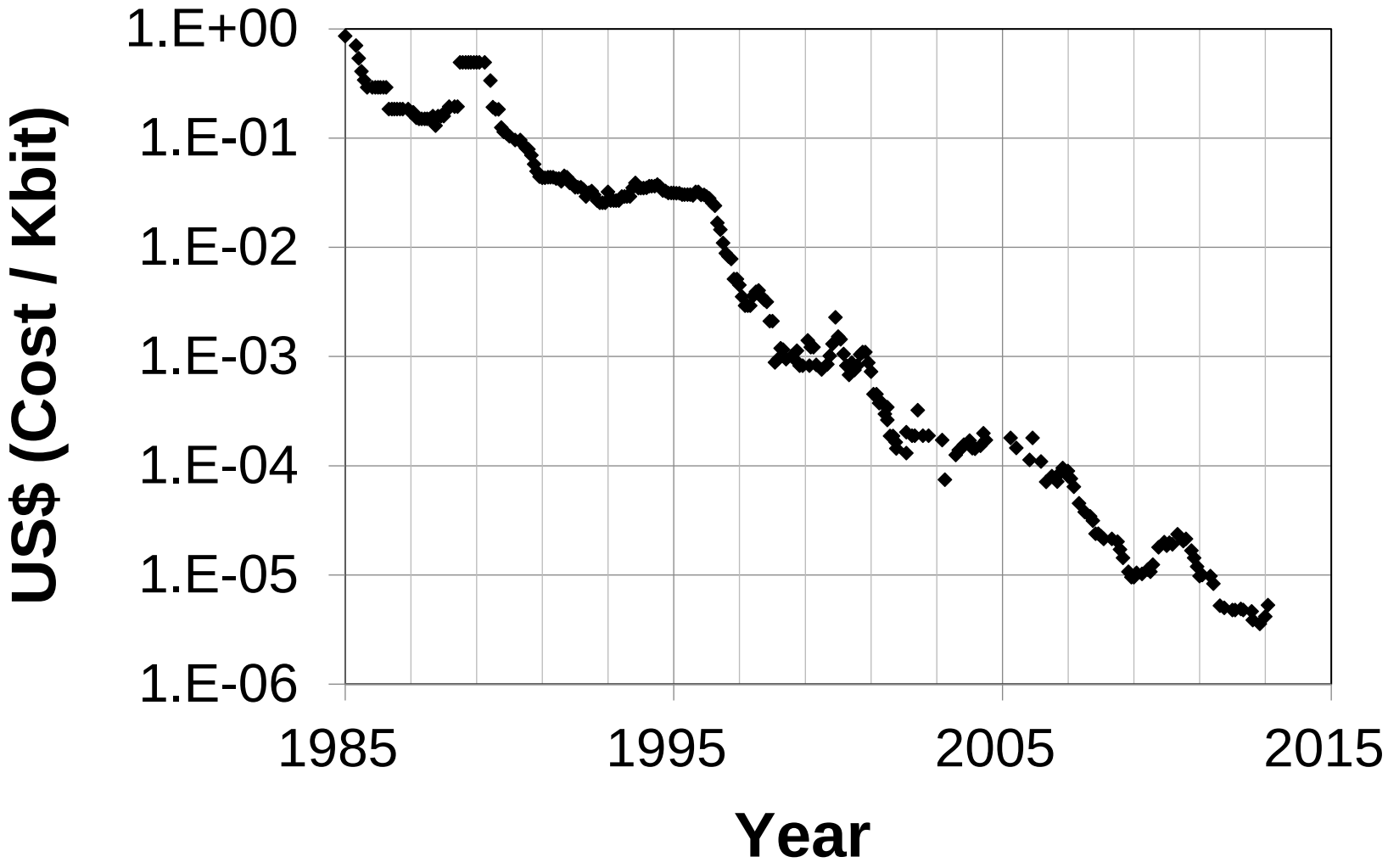


Offsetting wafer cost ($/mm^2) with density (mm^2/Tr) for 30% $/Tr scaling per node

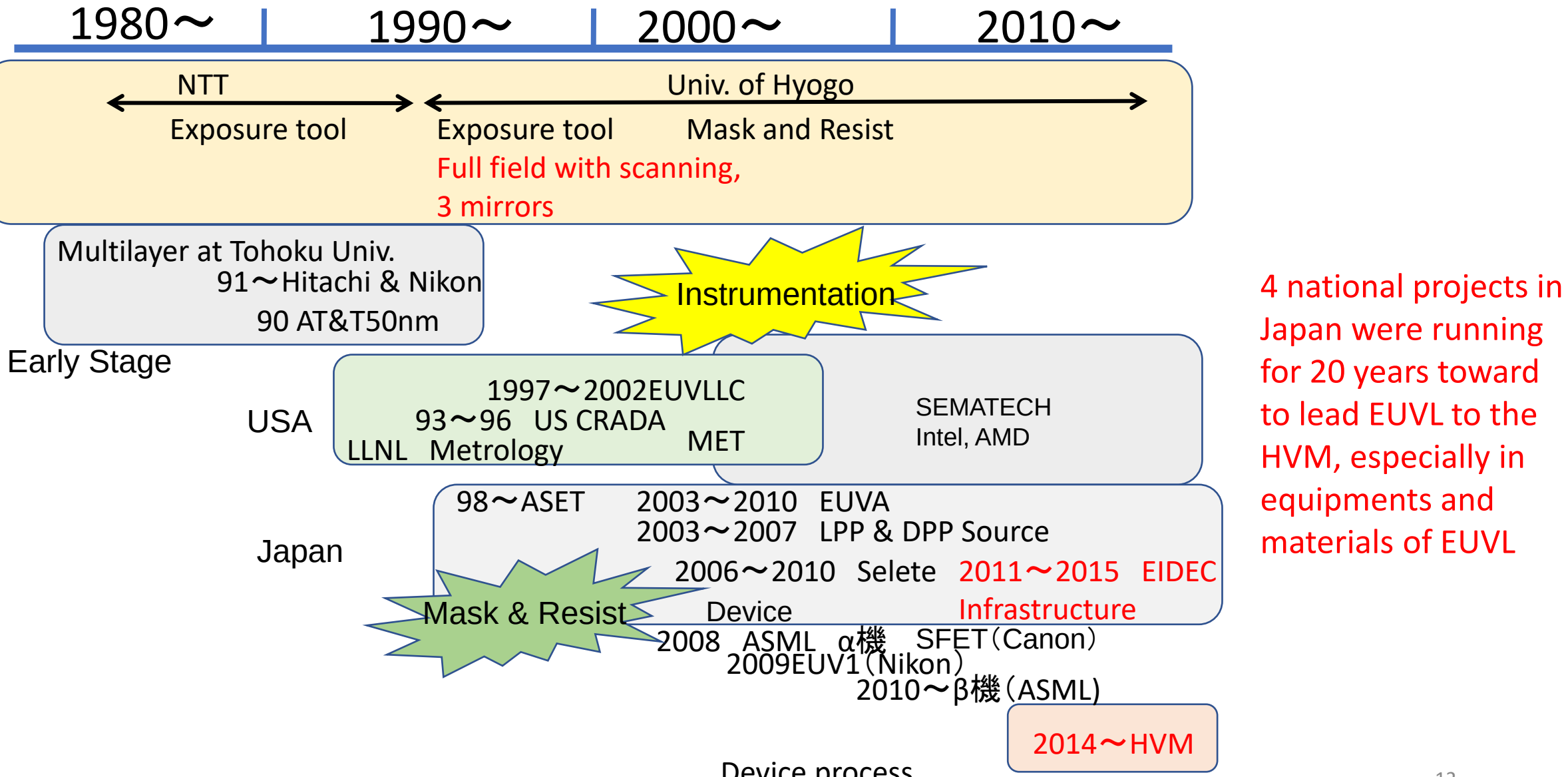
Reference: Intel, Bill Holt, ISSCC 2016

Embedded Systems and Innovation Technologies for IoT Applications, Ali Keshavarzi. IEDM 2016.

Memory Cost

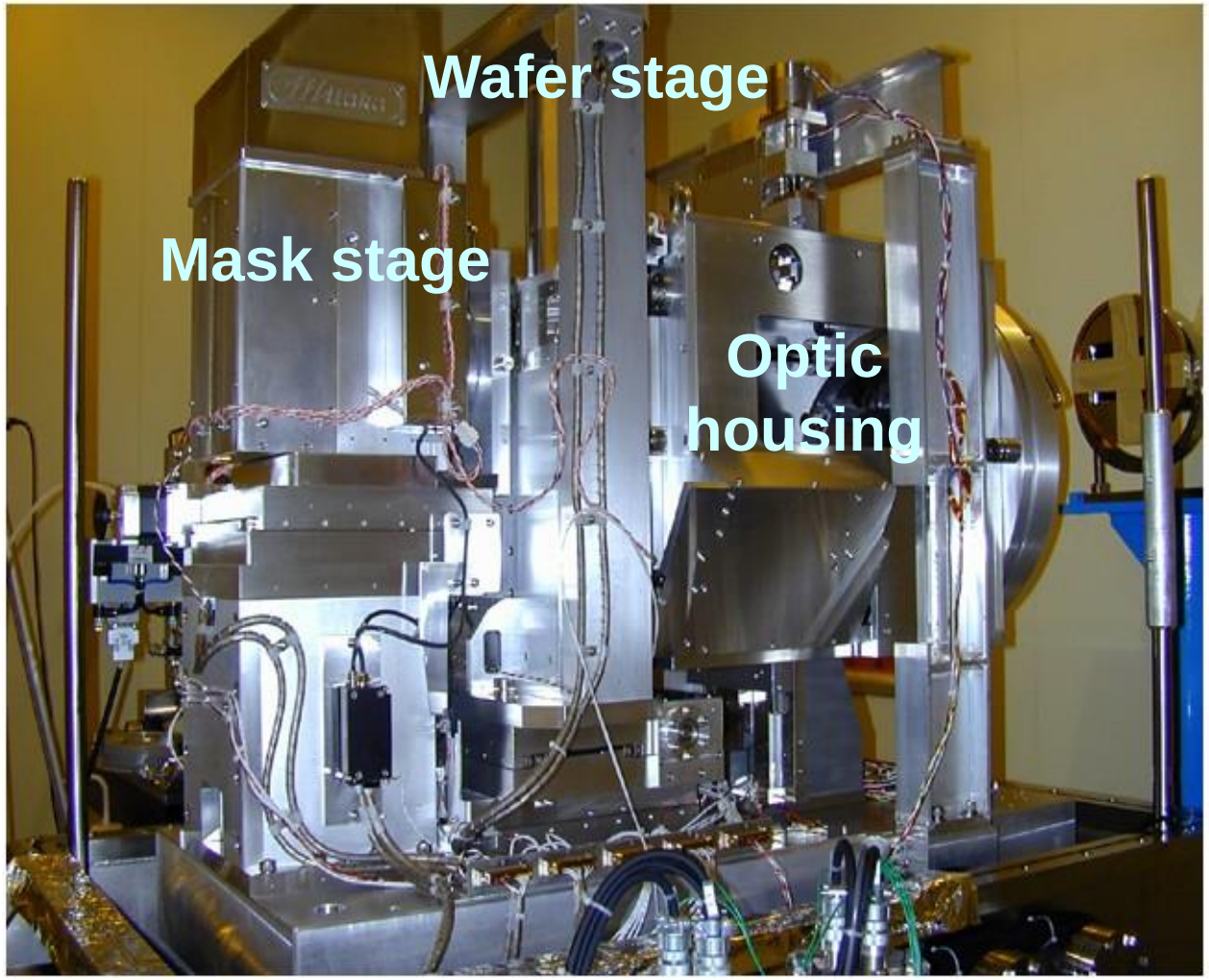

1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
US$ (Cost / Kbit)
1985
1995
2005
2015
Year

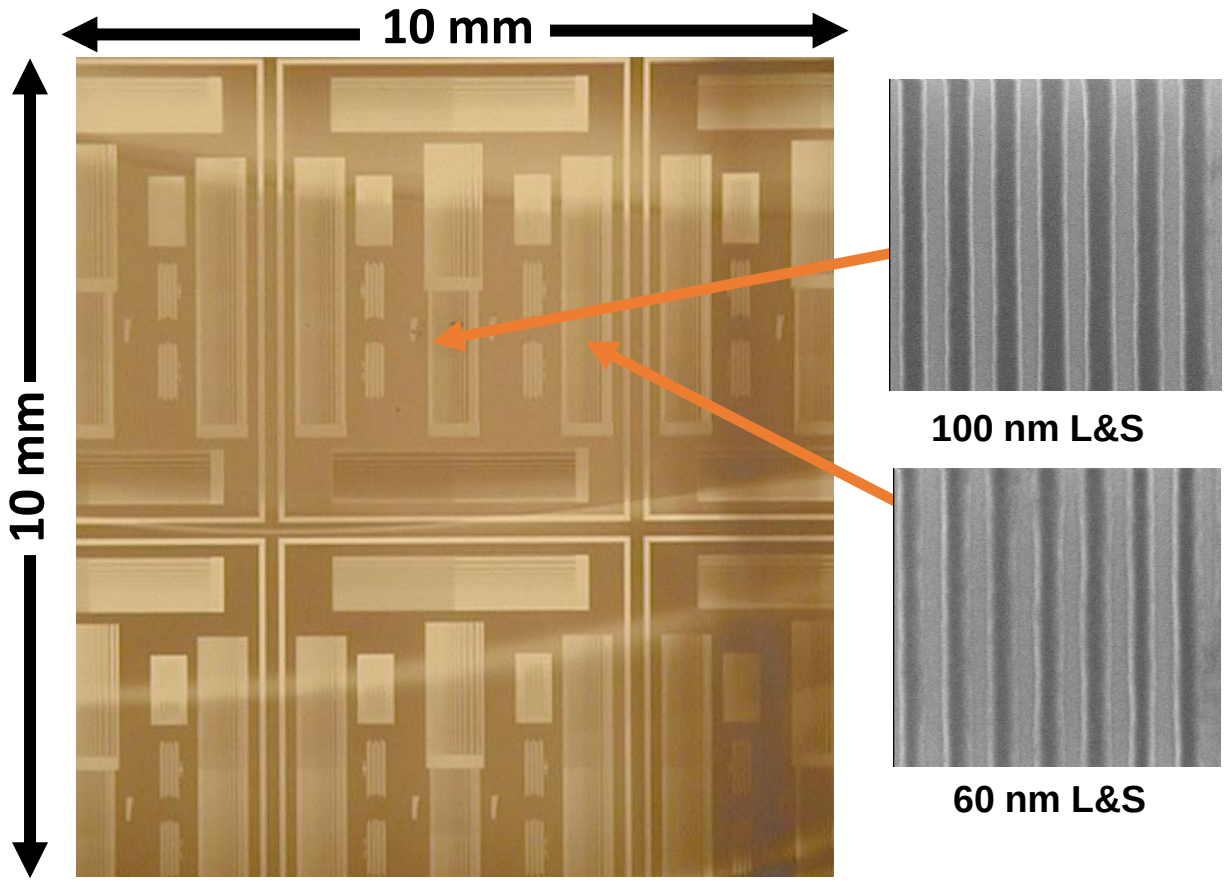
History of National Project in Japan and US



4 national projects in Japan were running for 20 years toward to lead EUVL to the HVM, especially in equipments and materials of EUVL

60 nm L&S pattern in large exposure area (World 1st) by ETS-1



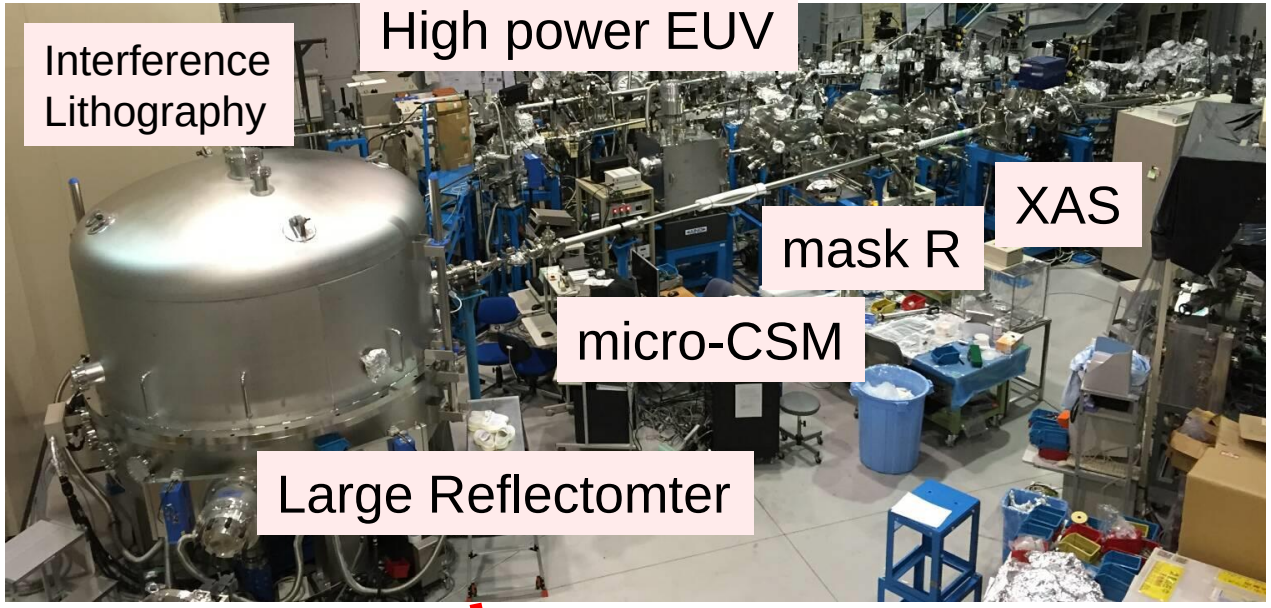


T. Watanabe, H. Kinoshita, K. Hamamoto, M. Hosoya, T. Shoki, H. Hada, H. Komano, and S. Okazaki, “Fine pattern replication using ETS-1 three-aspherical mirror imaging system,” *Jpn, J. Appl. Phys.,* **41** (2002) 4105-4110.

Center for EUV Lithography

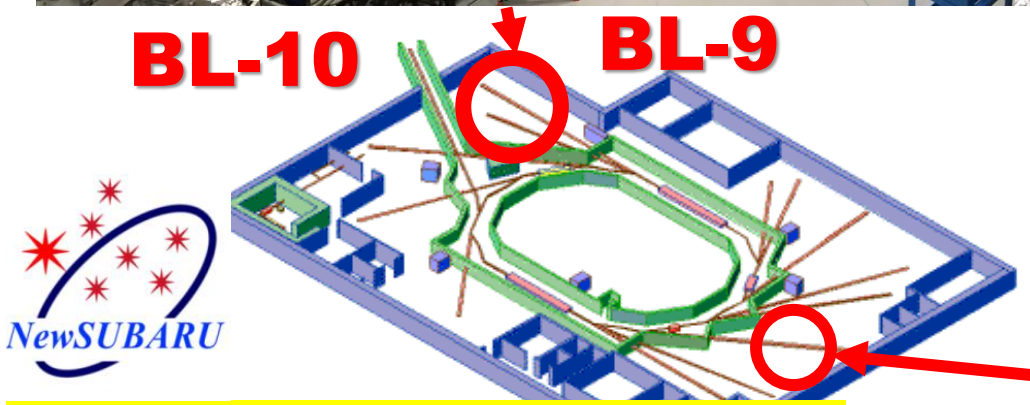
NewSUBARU Synchrotron Radiation Facility

in SPring-8 site



1) Resist
2) Mask
3) Large reflectometer of Collector mirror for EUV light source
4) Pellicle

Microscopes (EUVM)
Resist EUV Sensitivity



EUV & Soft X-ray

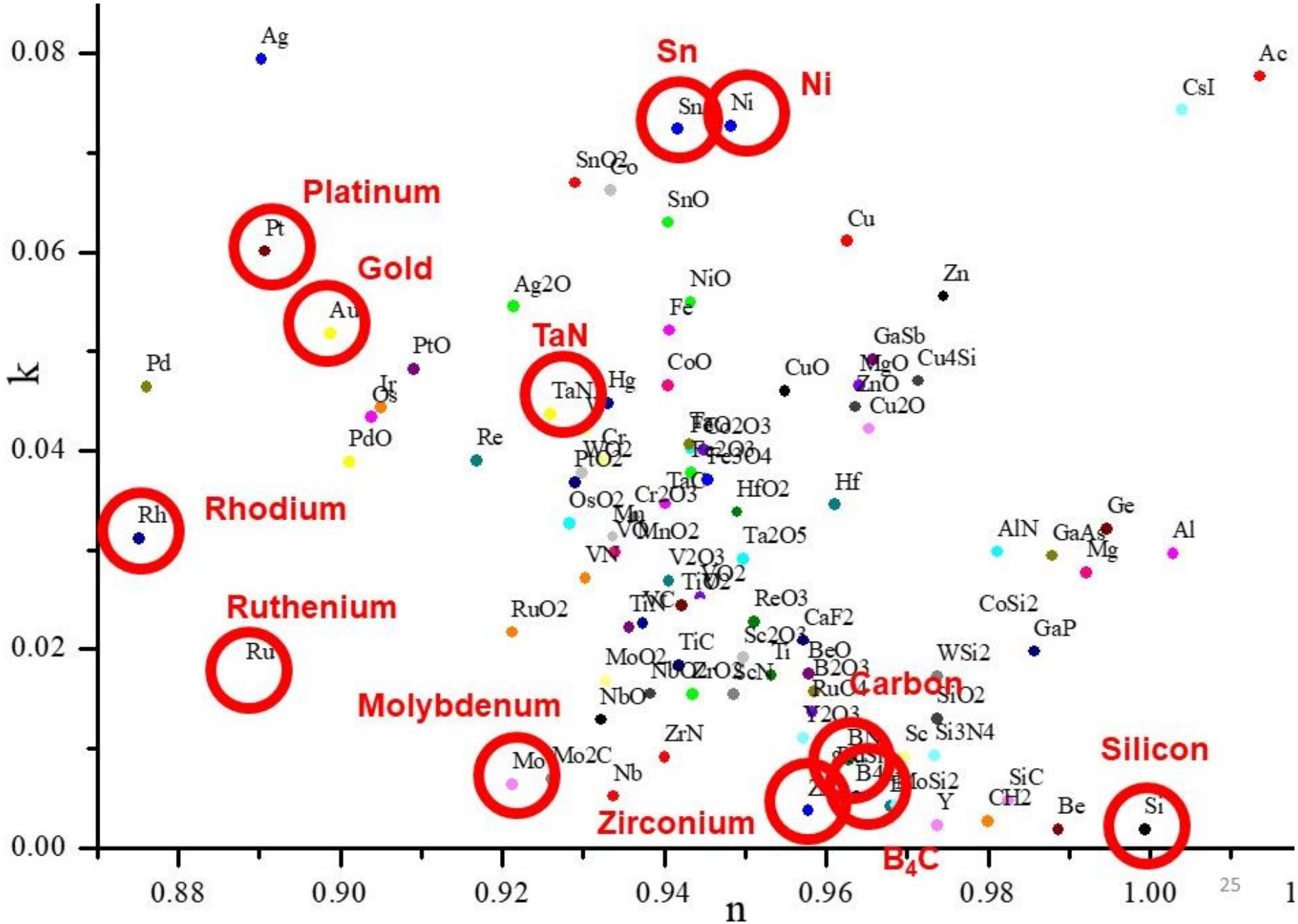
BL-3

Three Beamlines for EUVL

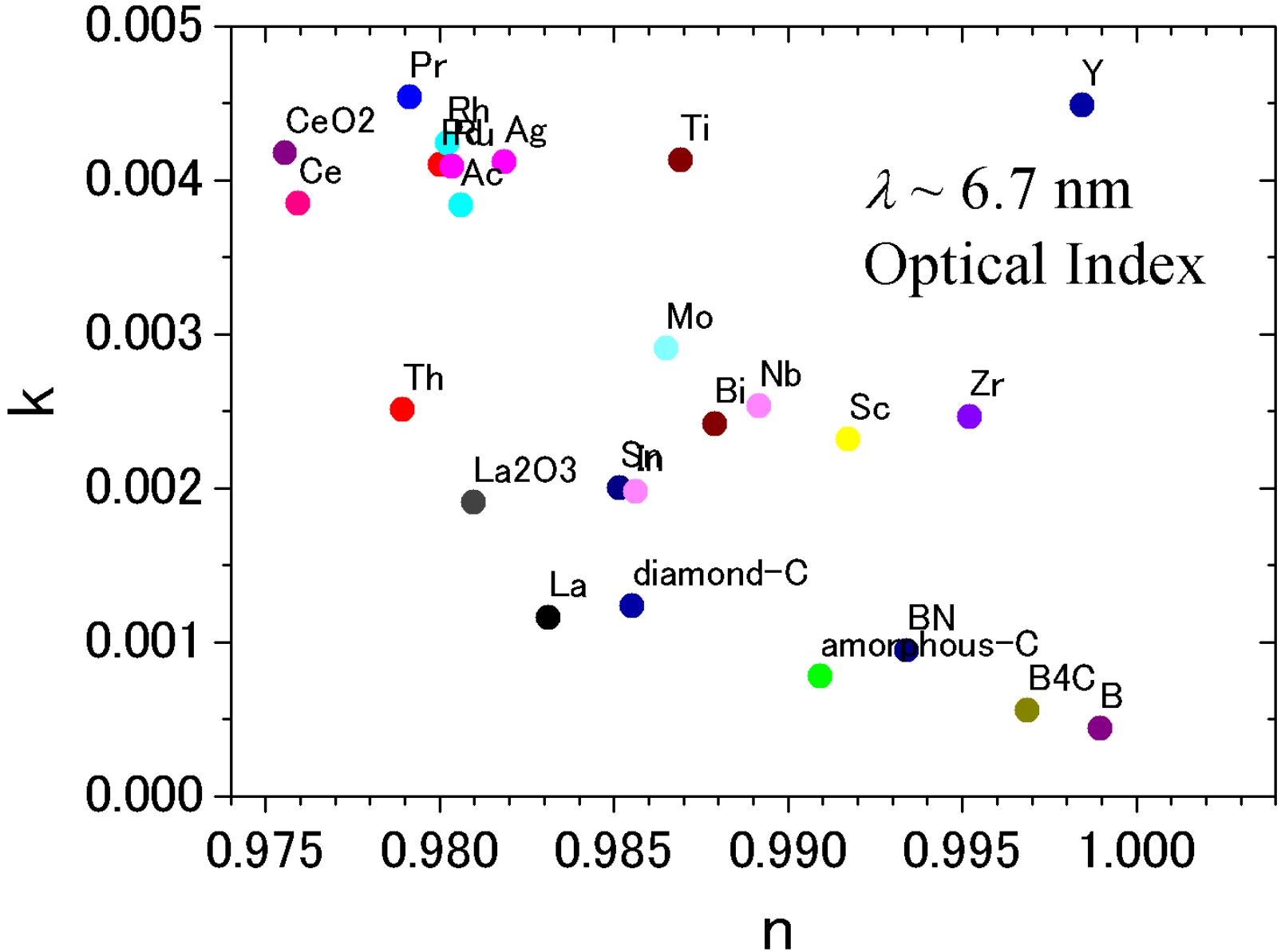
Continuing Advanced Lithography Now and in Future

Next Generation Technology	First Possible Use in Mfg.	22Feature Type	Device Type	Key Challenges	Required Date for Decision making
EUV Single Patterning	2018	22 to 24 nm hp CH/Cut Levels back end metals at 18nm hp LS	“7nm” Logic Node	-Pellicle -Actinic mask patterned mask inspection -Resist speed combined with LER and Stochastics -shot noise	Product Evaluation Completed
EUV Double Patterning	2022	12nm hp LS	“3nm” Logic Node	-Tolerance, EPE, and Overlay	2021
EUV high NA	2025	10.5nm hp LS	“2.1nm” Logic Node	-Stitching of two mask patterns -Shot noise	2024
EUV new wavelength	2028 ?	8nm hp LS ?	“1.5nm” Logic Node	-EUV source power -Resist material -Actinic blank and patterned mask inspection	2030
NanoImprint	2019	20 nm lines and spaces 20 to 30nm contact holes	3D Flash Memory	-Defectivity -Overlay -Master Template fabrication and inspection <20nm -Defect repair -Mass-production capacity	Product Evaluation Completed
DSA (for pitch multiplication)	2022	Contact hokes/cut levels for logic. Possibly nanowire patterning	“3nm” Logic Node	-Pattern Placement -Defectivity and defect inspection -Design -3D Metrology	2021

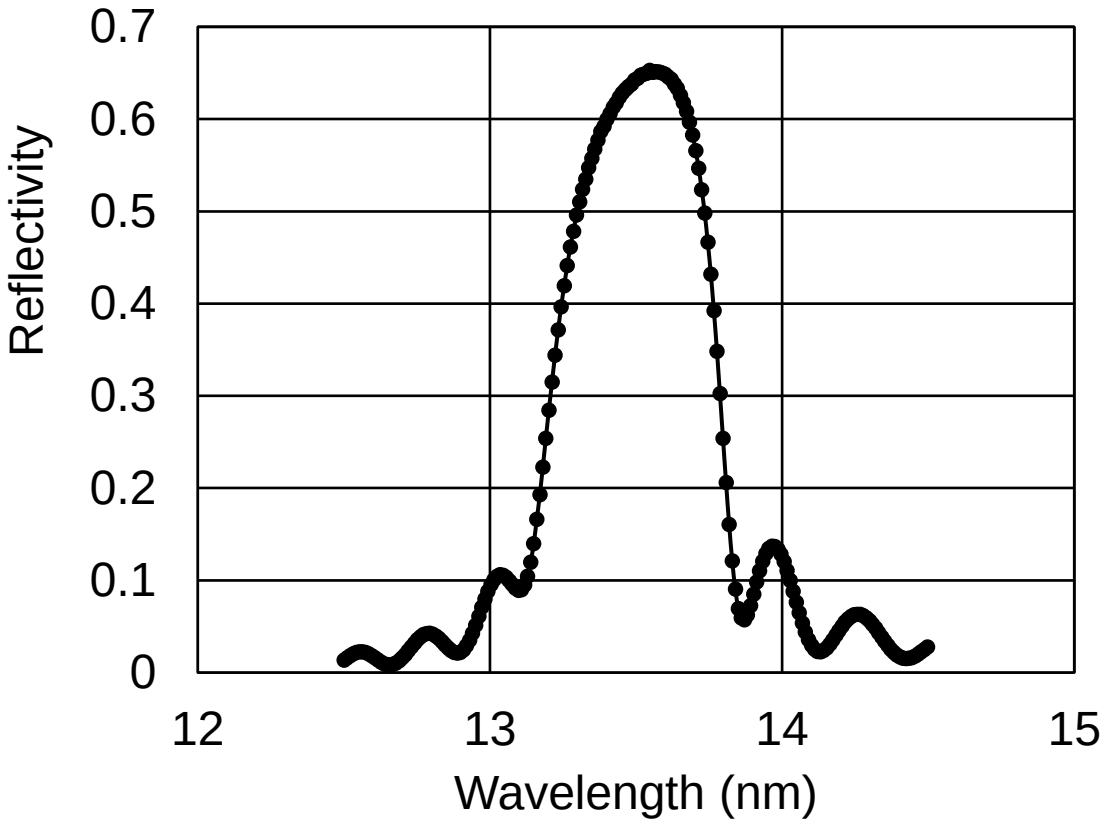
n & k values @λ=13.5 nm



Candidate of ML materials for BEUV （λ=6.7 nm）

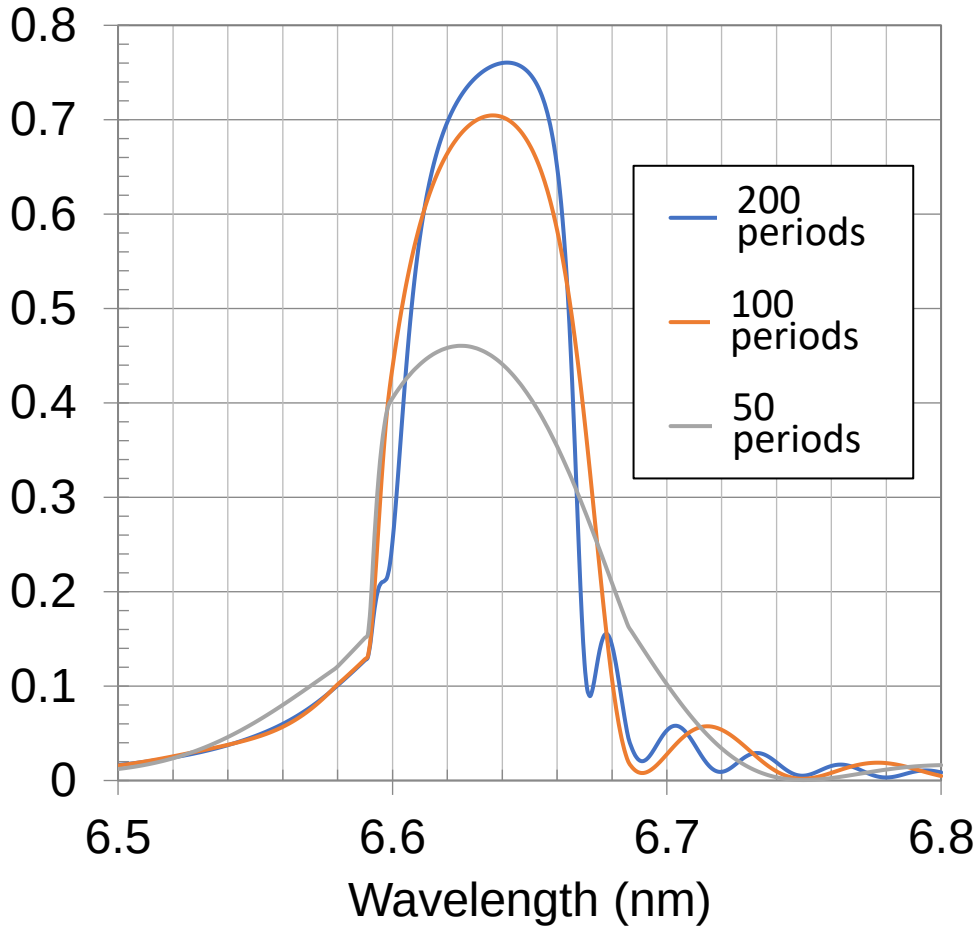


Reflectivity of Mo/Si Multilayer



4% bandwidth

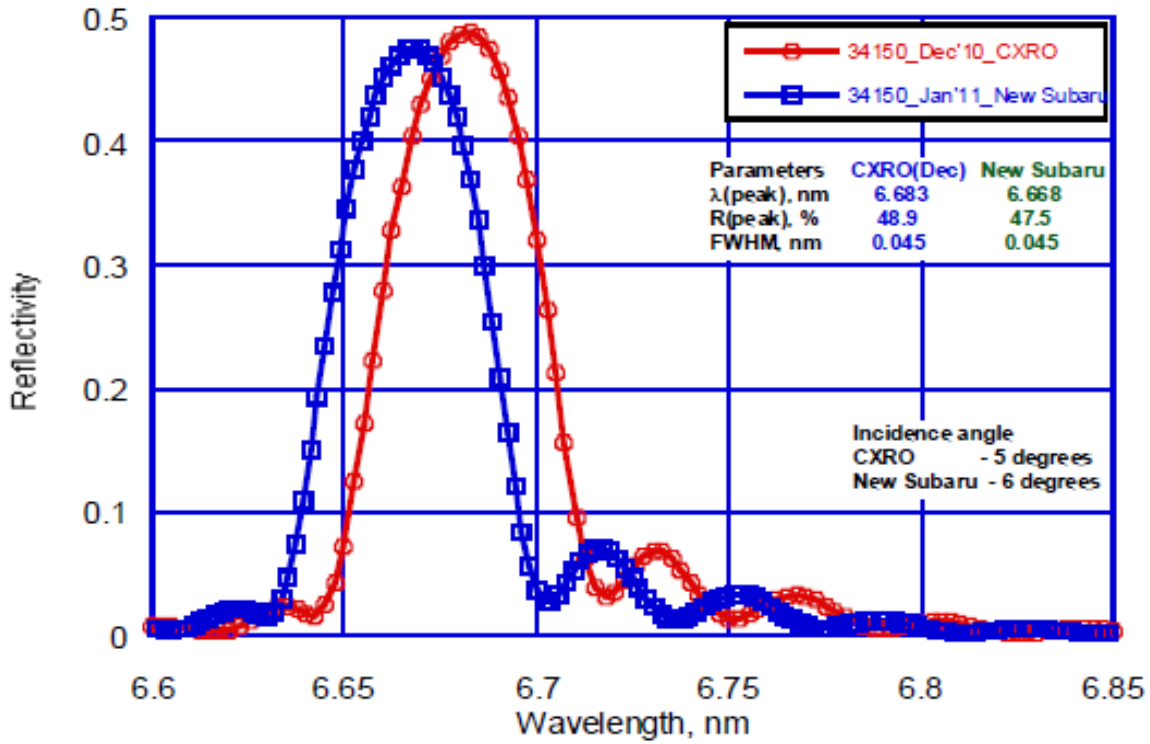
Reflectivity of LaB Multilayer



<1% bandwidth

Next Generation EUVL Optics for 6.X nm

- Achieved the highest measured reflectivity to date, actively developing multilayers to their theoretical limit ~ 70%



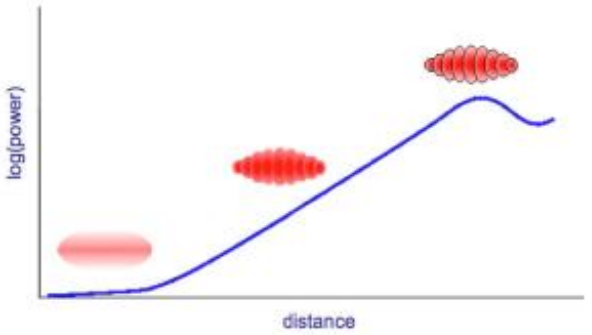
By courtesy of Rigaku

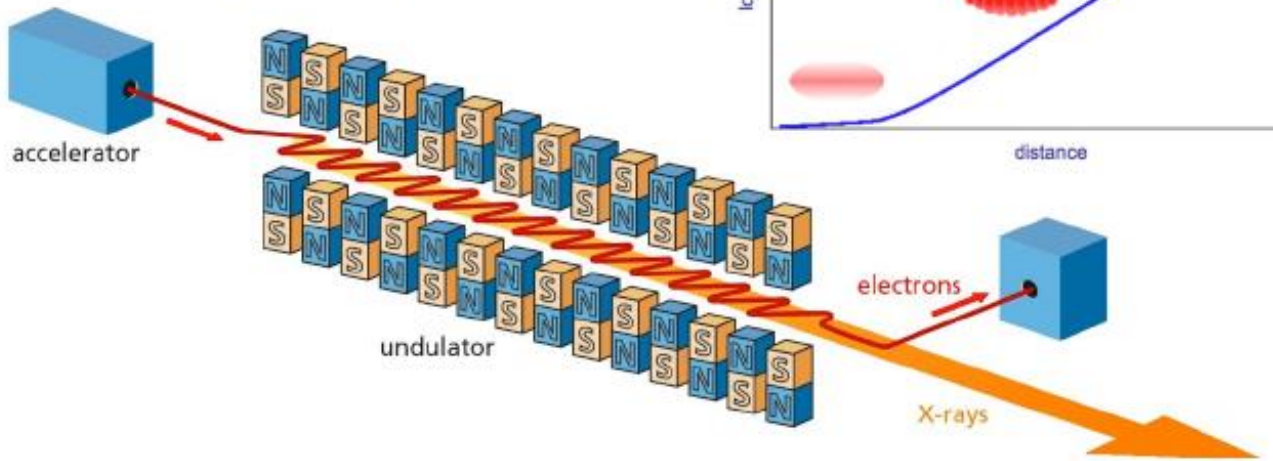
FEL for EUV Light Source

FEL is a clean light source

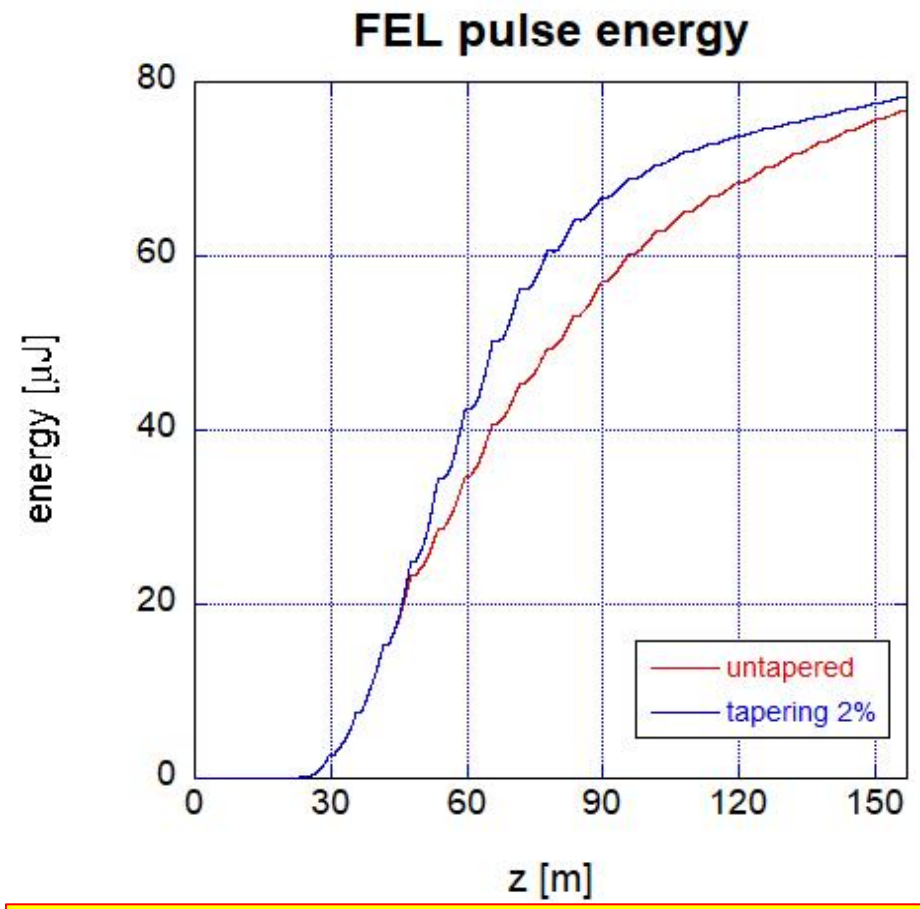
- In Free Electron Laser relativistic electrons travel through the undulator magnet in vacuum and generate X-rays
- No contamination
- Minimal thermal load
- Directional output
- Scales to high duty cycle

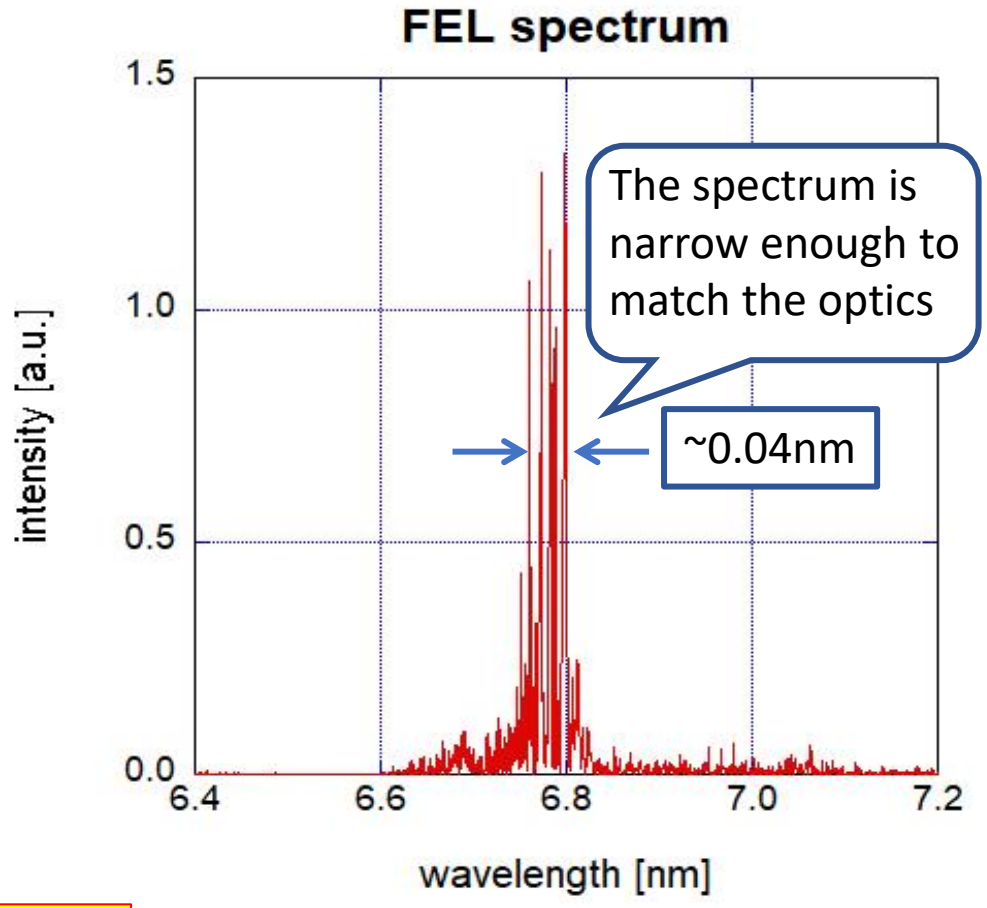
high quality e-beam = microbunching and coherent amplification





Recent study about the power and spectrum at BEUV





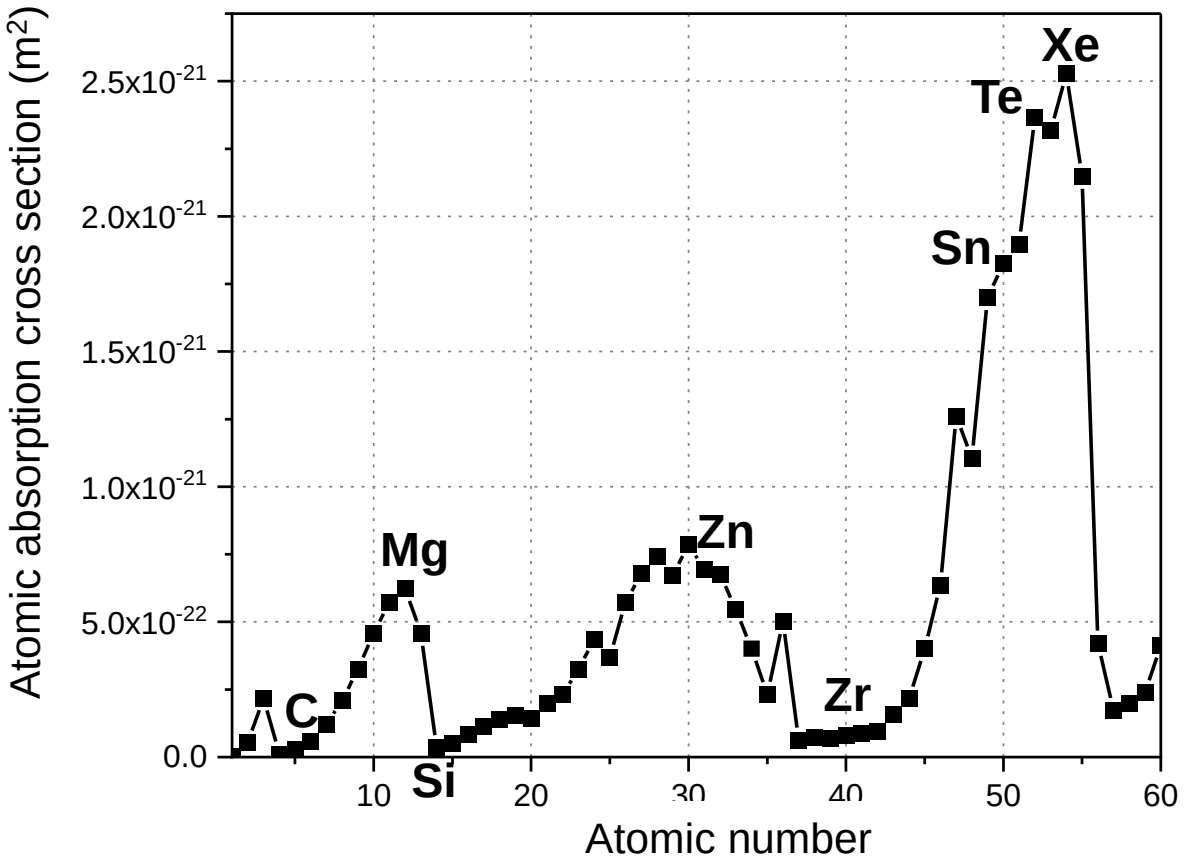
FEL power with 2% tapering:
12.7/25.4 kW @ 9.75/19.5 mA (162.5/325 MHz)

$\Delta\lambda/\lambda = 6 \times 10^{-3}$

Accelerator Parameters: E_{acc} = 1131 MeV $(800 \times \sqrt{2})$,
The other conditions are almost same to these of EUV-FEL

Achievement of high sensitivity EUV resist

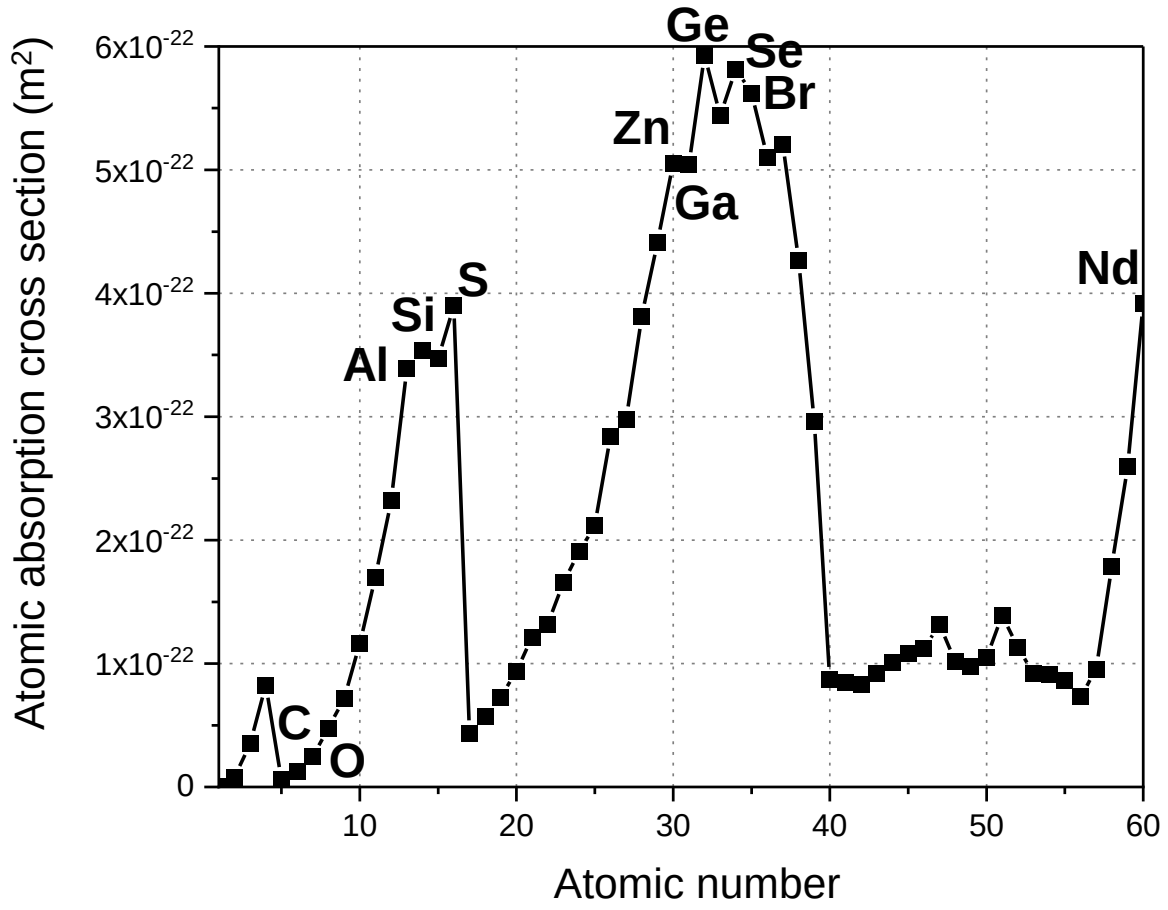
Atomic absorption cross section @λ = 13.5 nm



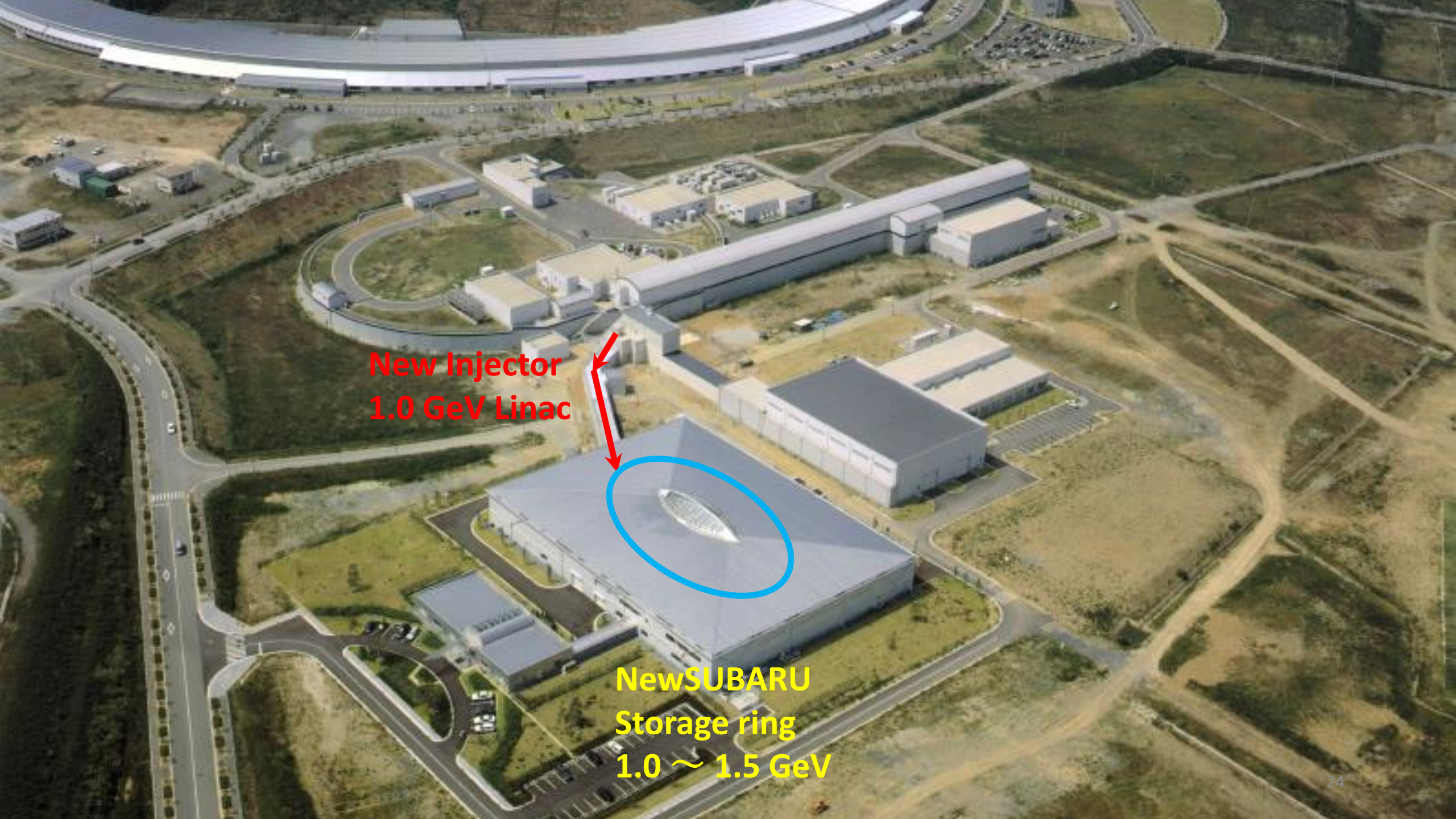
Since the EUV absorption of EUV resist increased, the secondary electron yield can increase.

Achievement of high sensitivity BEUV resist

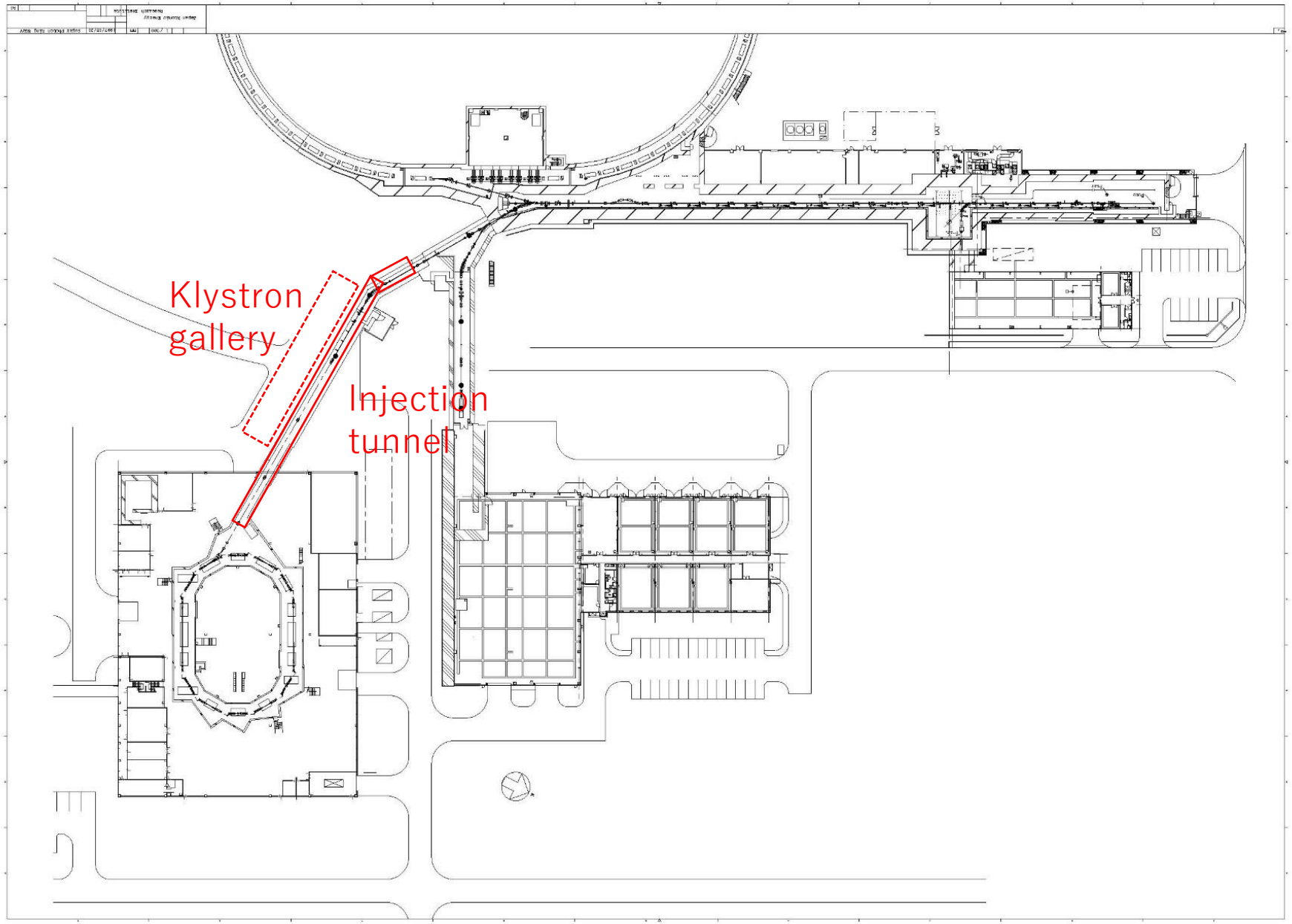
Atomic absorption cross section @λ = 6.7 nm



Since the BEUV absorption of BEUV resist increased, the secondary electron yield can increase.


New Injector
1.0 GeV Linac
NewSUBARU
Storage ring
1.0 ～ 1.5 GeV


NewSUBARU synchrotron
light facility
New 1.0 GeV injector
Klystron gallery


Klystron
gallery
Injection
tunnel

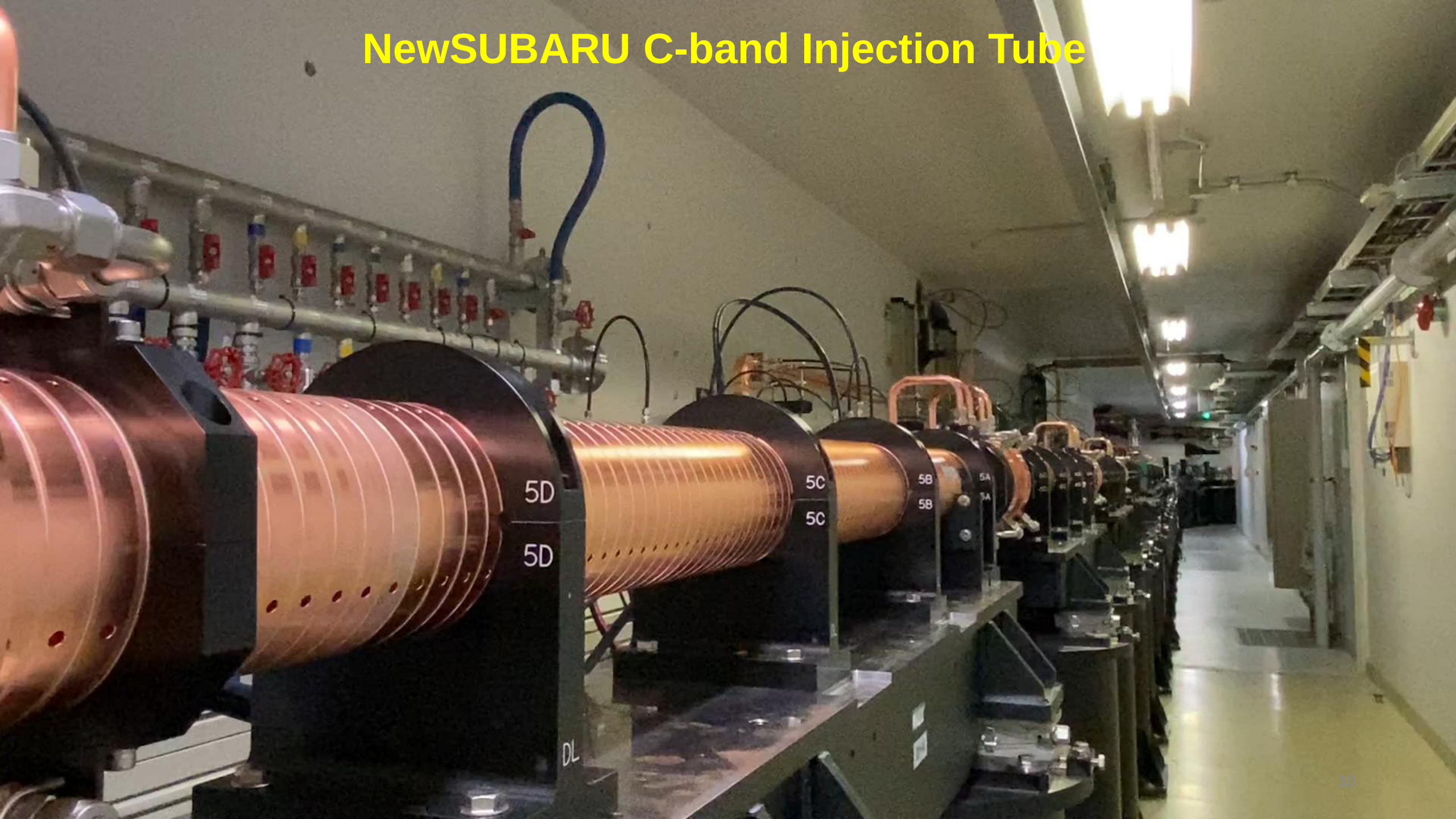
New Injector Construction Program

2016		Starting the program
2018		Construct the Klystron Gallery along the electron beam transport tunnel
2019		E-gun electric power supply and RF systems of s-band (3GHz) and c-band (6GHz) were installed in the Klystron Gallery
2020	Aug. to Dec.	New injector installation
2021	Jan.-April	New injector tunning
2021	April 20th	Commissioning has been started

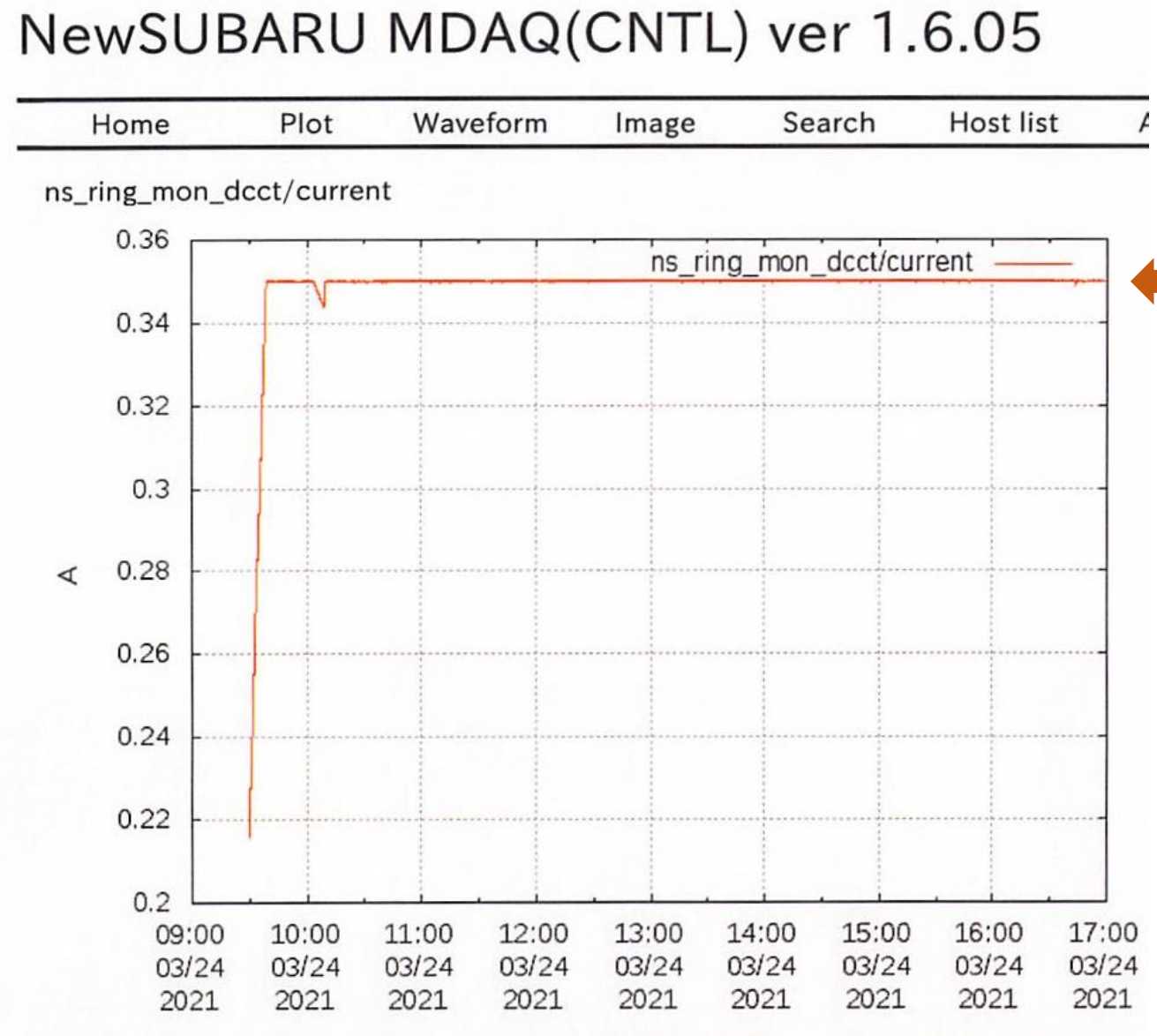
Klystron Gallery

New injector installation

NewSUBARU C-band Injection Tube



NewSUBARU Typical Operation Beam Condition



Stable operation of 350 mA beam current by the continuous injection @ 1.0 GeV

(Conventional operation: 300 mA)

Summary

1. The necessity of the Advanced lithography is introduced.
2. Since 1995, EUV R&D has been started at the middle size NewSUBARU synchrotron light source of University of Hyogo, which is the largest synchrotron facility operated by university in Japan.
3. Up to now, many significant technology research and development in EUV lithography were done by our research group. The showcase for resolving EUVL technical issues will be presented for the wide range technologies including resist, mask, pellicle, optical element evaluation, and so on.
4. Not only EUV but also BEUV R&D program will continue to resolve the technical issues for the transformation to HVM.
5. For the BEUV, BEUV-FEL is required.
6. New Injector for NewSUBARU Storage Ring installation has been completed and commission has started since April 20, 2021.
7. Many only-one EUV equipment are on operation at three EUV beamlines of NewSUBARU, and they opened for the EUVL users in worldwide.

Contact Email Address

If you have furthermore questions and requirements to update or renewal the tools to build up, please do not hesitate to contact to the following email address.

Email address: takeo@lasti.u-hyogo.ac.jp

Thank you for your kind attention!!