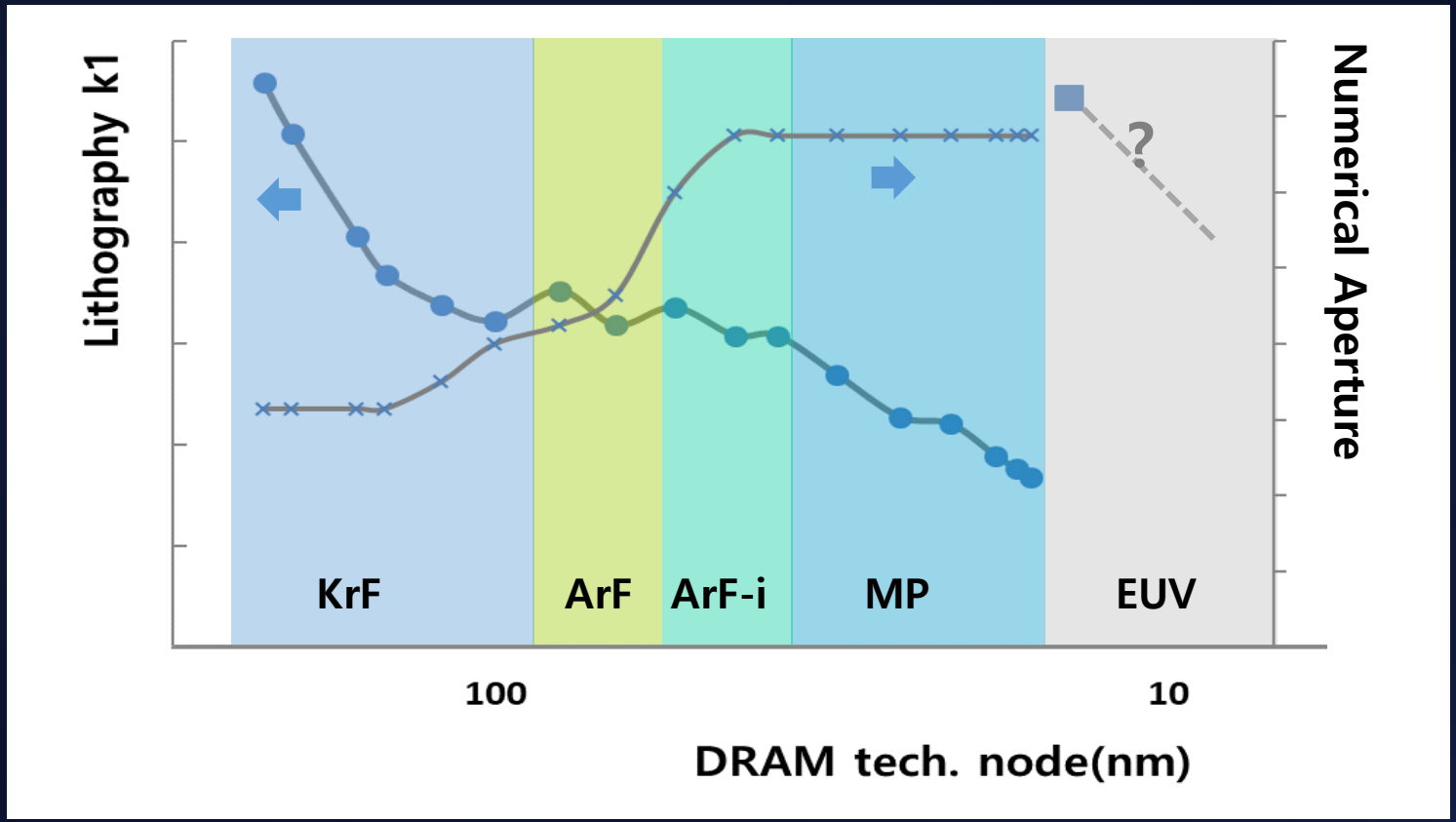
Potential of EUV for high volume manufacturing of DRAM

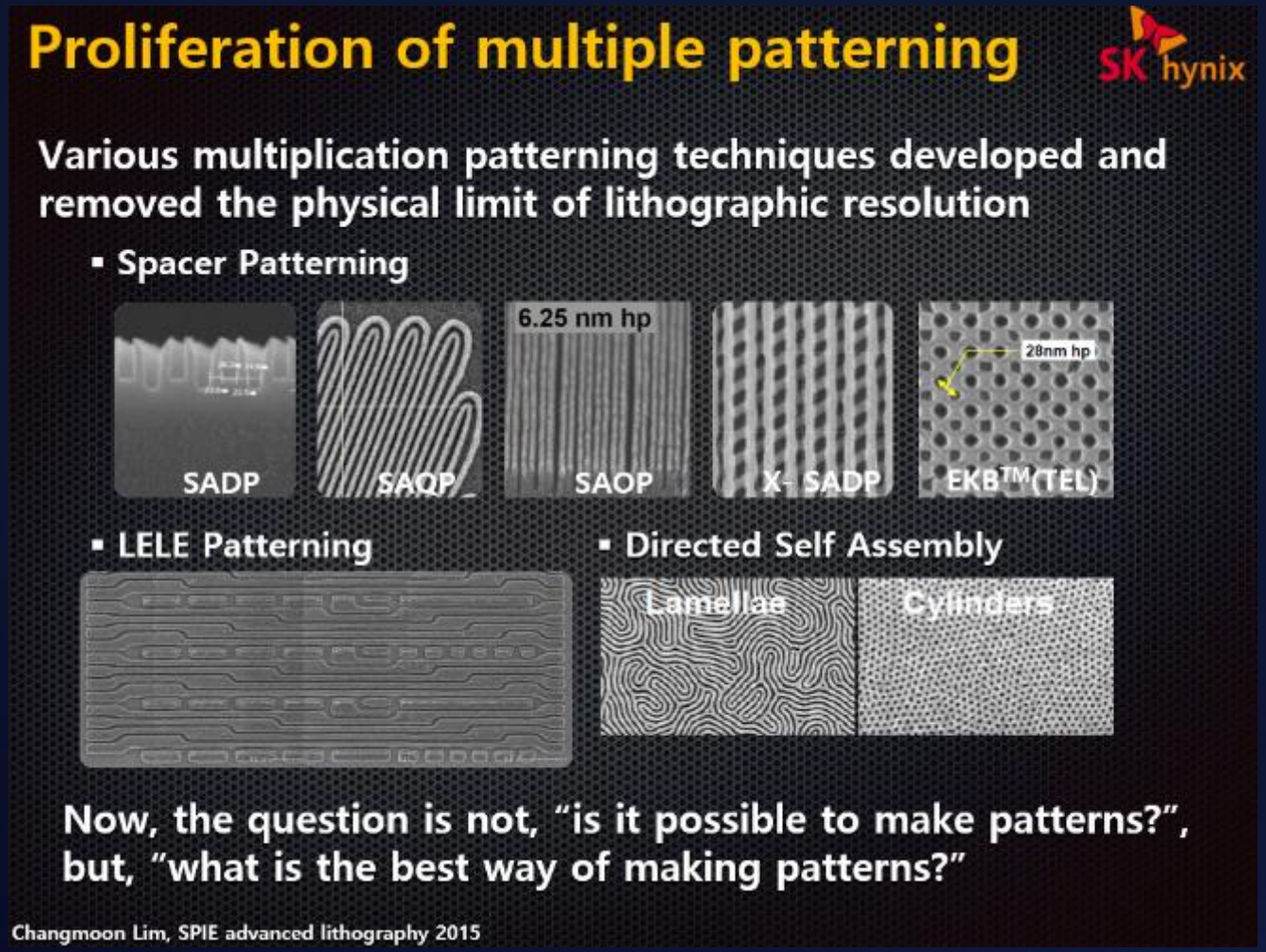
Changmoon Lim
Research fellow/ SK hynix

Traditionally, k1 race has driven by DRAM industry



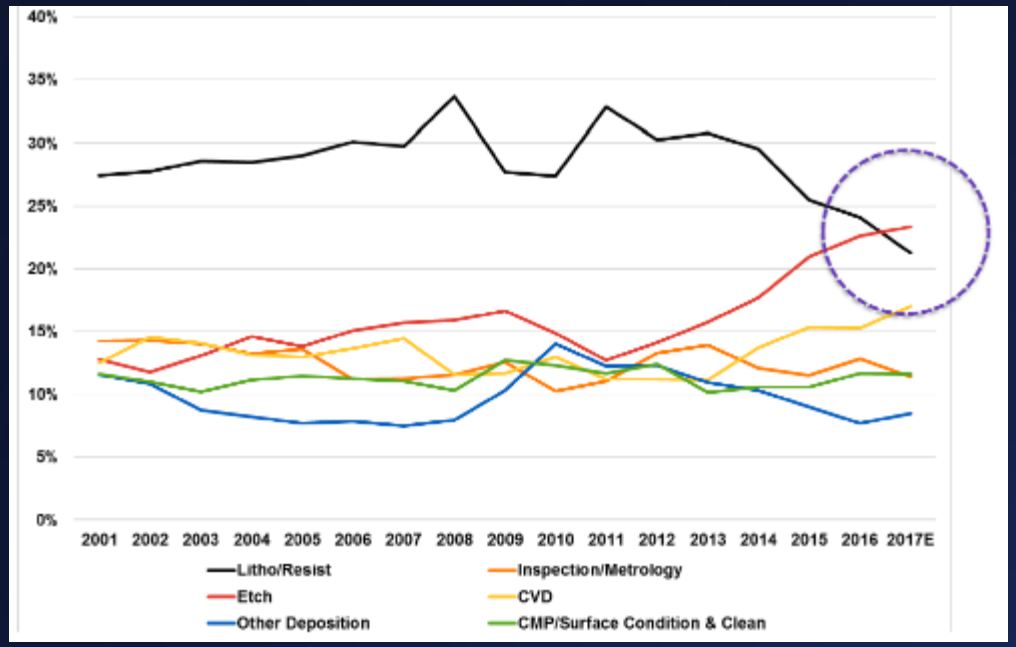
- ✓ Scaling competitiveness has been a key success factor in DRAM industry
- ✓ Generally agreed understanding exists on the k1 limit of 193nm immersion single patterning, but, much questions left on EUV still

Multiple patterning and era of etch technology



※ presentation in SPIE AL 2015

- Fab equipment market share by type



※Source: SEMI/SEAJ, WWSEMS

Lithography era will return with EUV taking off

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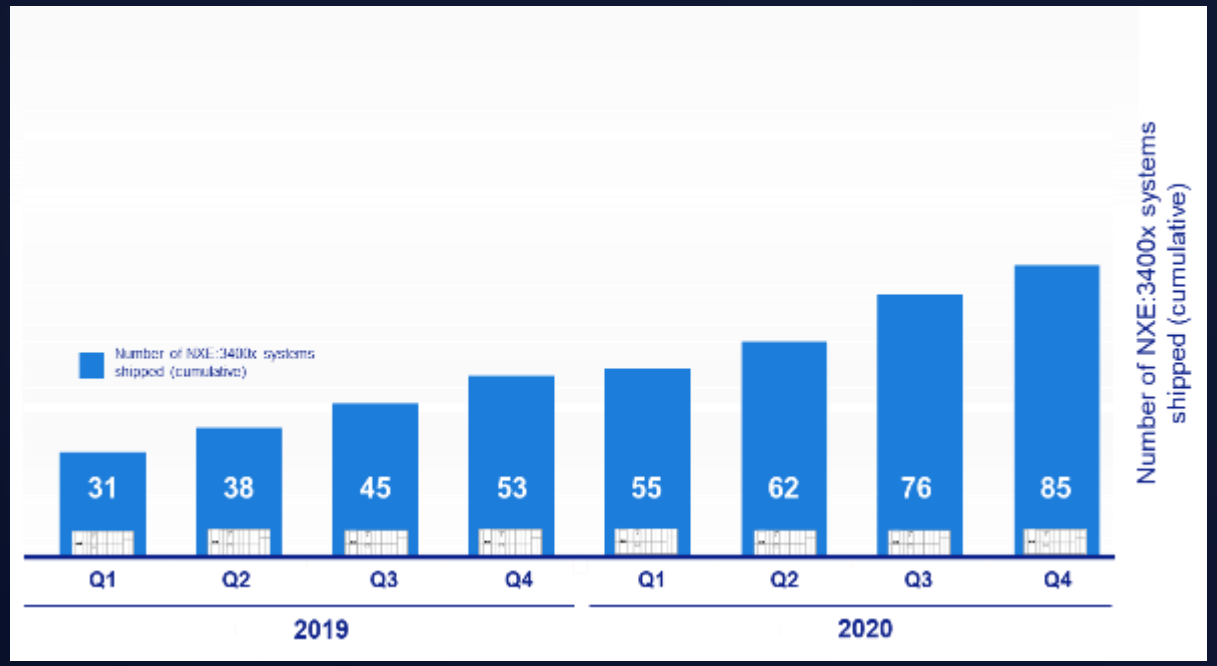
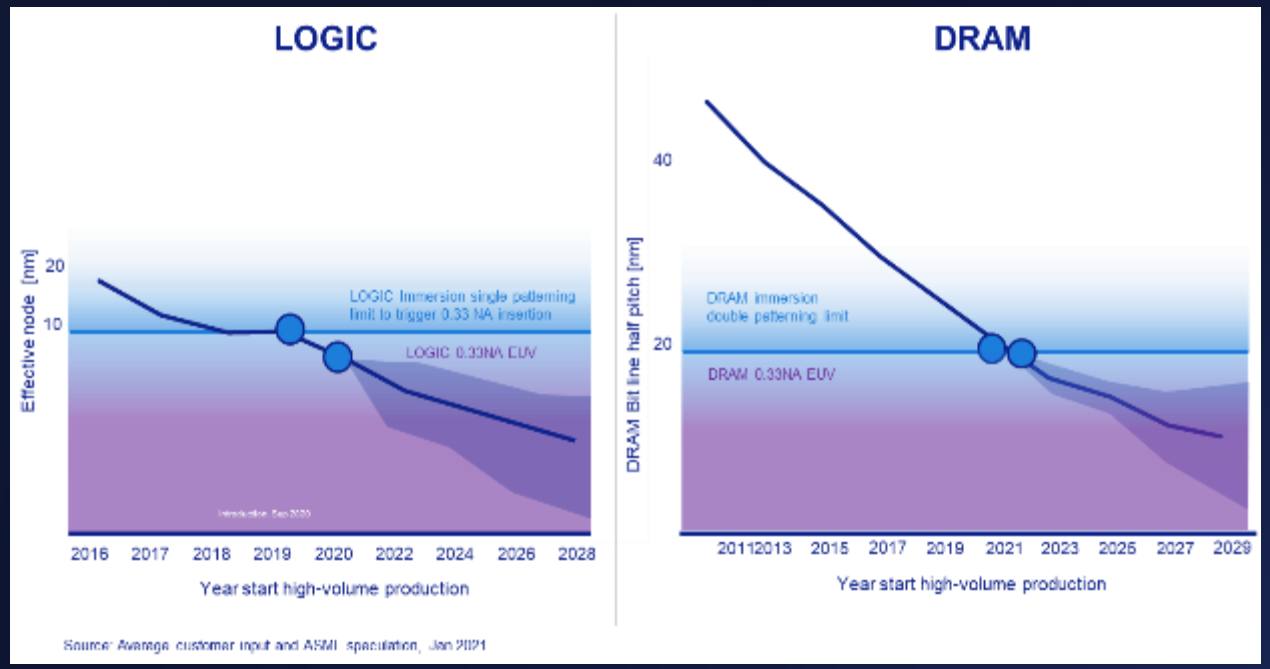
- Total number of shipped EUV systems



- EUV HVM trend

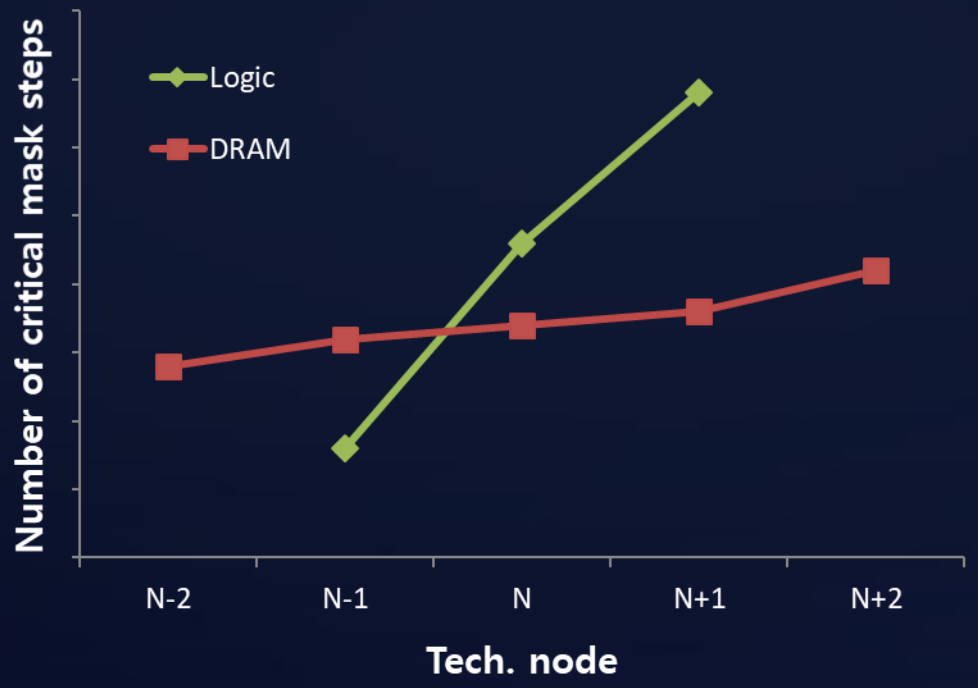


※Eric Verhoeven (ASML, SPIE AL 2021)0

✓ EUV adoption in logic and DRAM sector drives the returning of single patterning
✓ Later adoption in DRAM than logic doesn't mean that difference in design rule, there are more than what the node numbers tell…

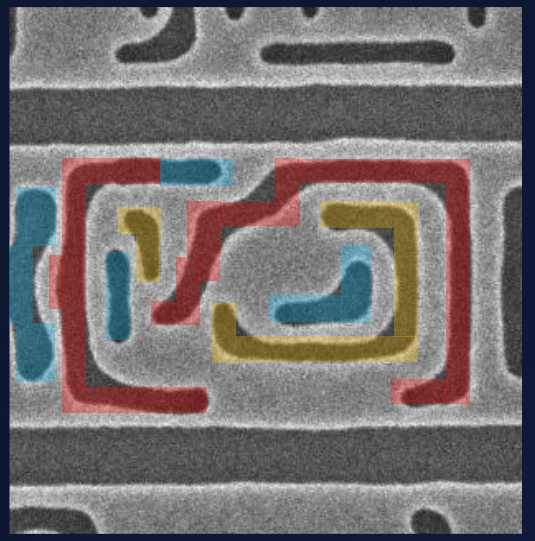
Why Logic more enthusiastic than Memory on EUV

- Number of immersion mask steps

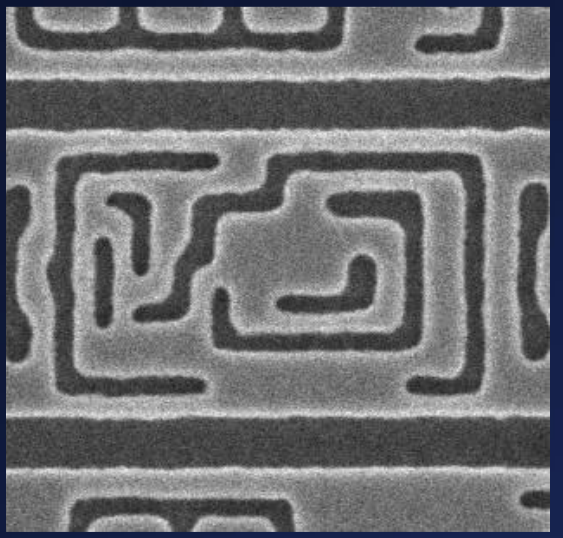


- Pattern fidelity provides design freedom

Multi-patterning



EUV single

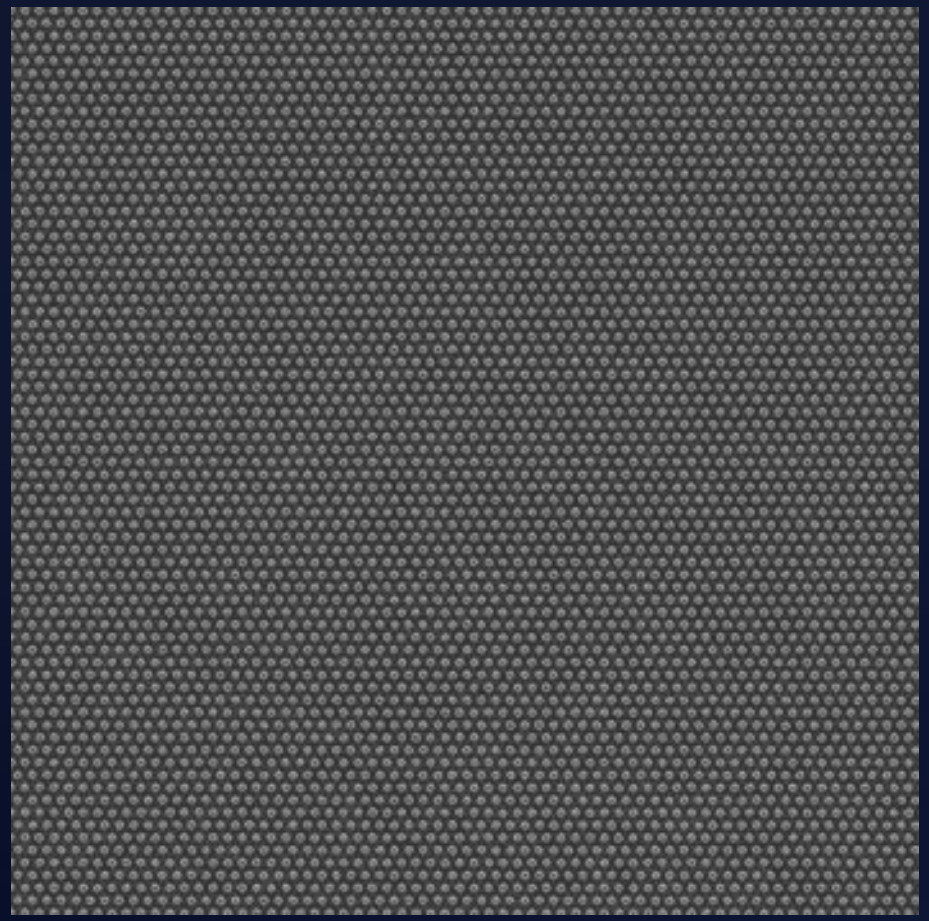


※ Source: IMEC

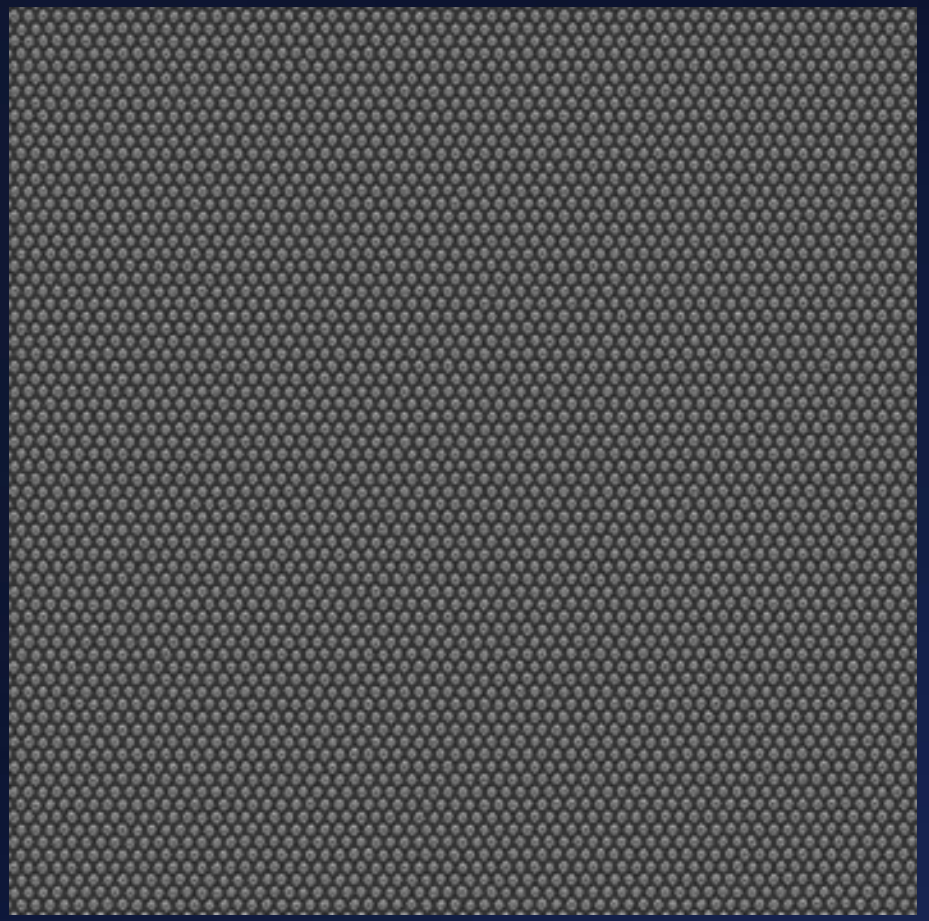
✓ Number of critical lithography steps increases moderately in DRAM without EUV
✓ EUV provides significant design freedom in logic compared to DRAM

Patterning of DRAM

- EUV single patterning



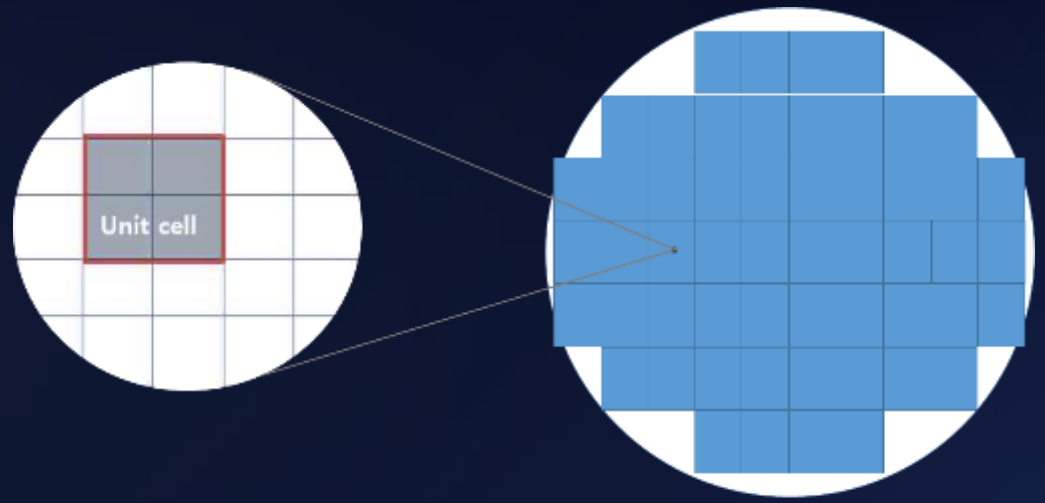
- ArF immersion multi patterning



✓ Memory patterns by immersion multiple-patterning almost identical to EUV, similar appearances and qualities

Value of lithography

Economic value of lithography
∝ Number of bits produced per unit time



$$\#\ \text{of bits on wafer} \sim \frac{\pi \times (150\text{mm})^2}{\text{gate pitch} \times \text{bit-line pitch}}$$

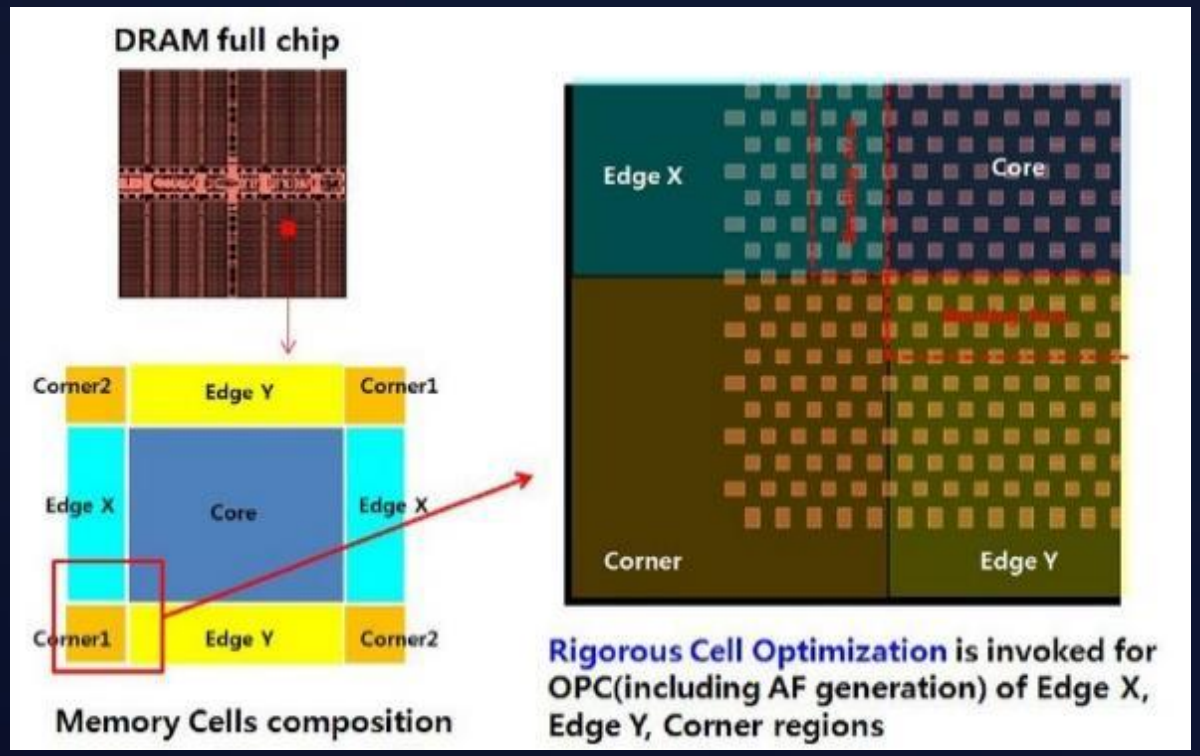
where, number of bits

$$\propto \text{Throughput} \times \text{bits on wafer}$$

(wafers/hour) (wafer area/ resolution^2)

DRAM patterns not always periodic

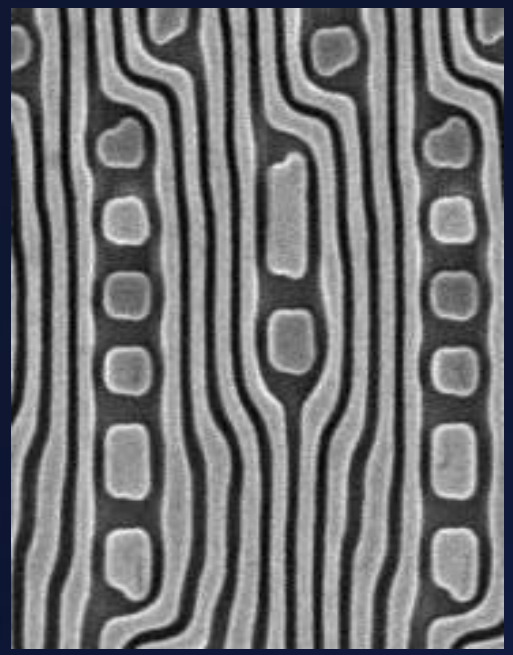
- Memory unit block architecture



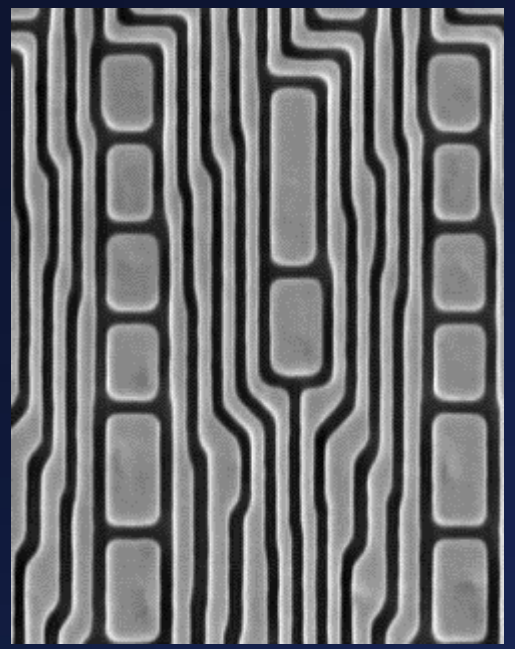
※ Jinhyuck Jeon(SK Hynix, SPIE AL 2014)

- Core and periphery patterns

Immersion DP

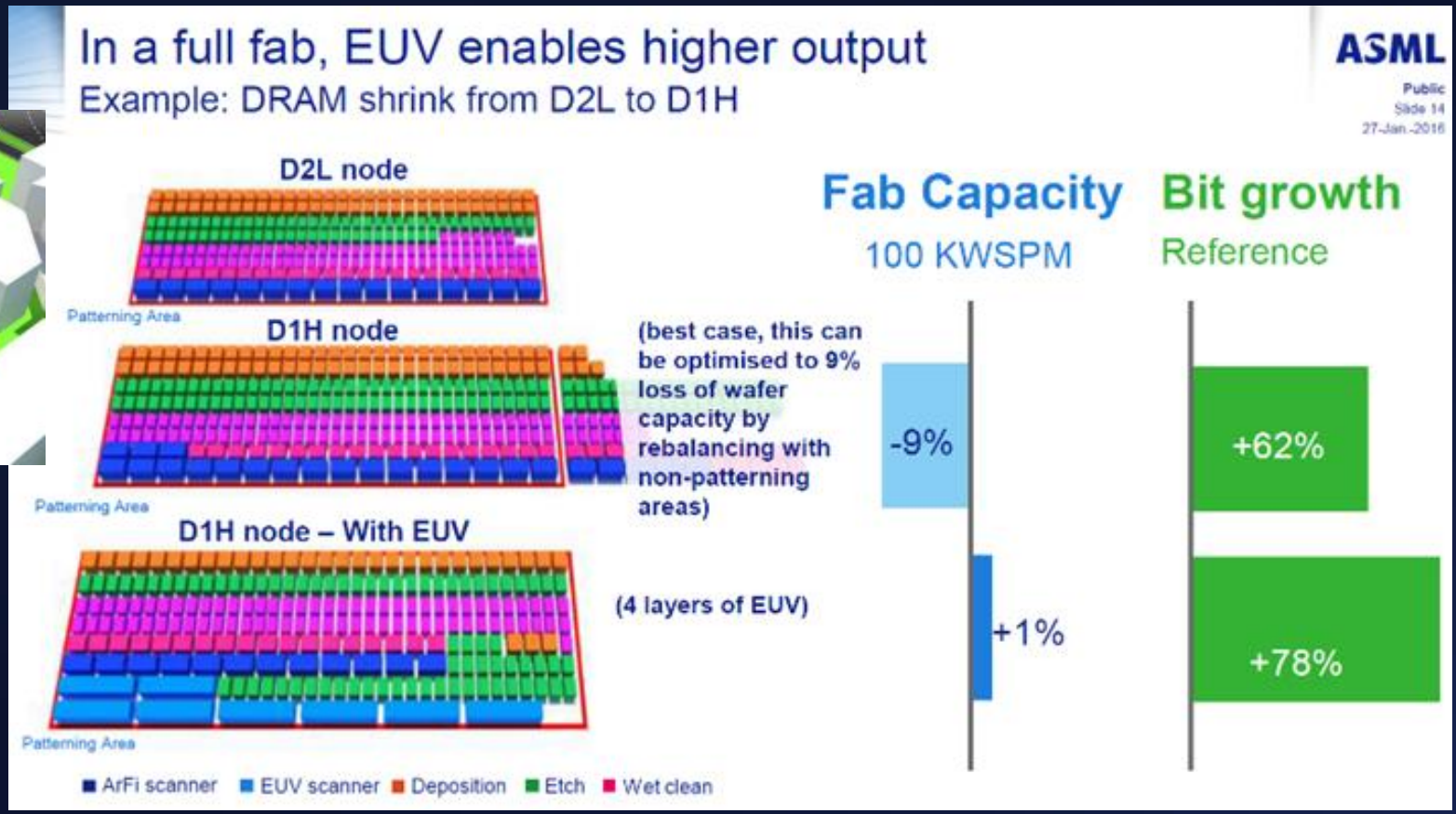


EUV SE



✓ Patterning challenge rises where periodicity is broken, such as in the edge of cell block and periphery area

Wafer fab; one of the most expensive real estate

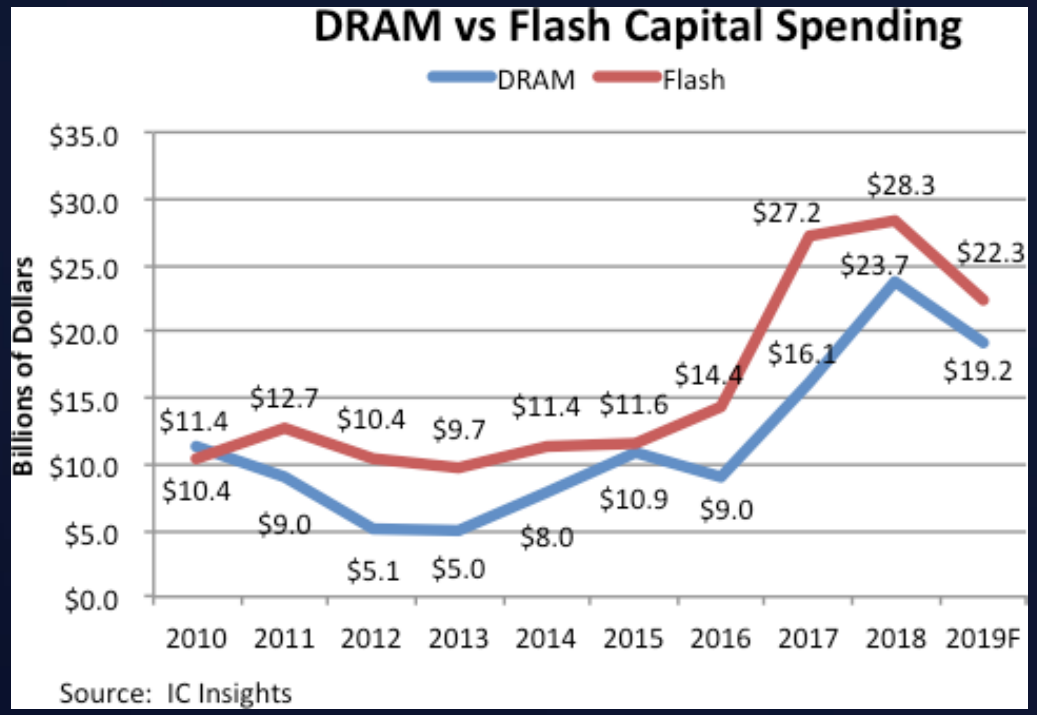


※ B. Sluijk (ASML, Semi Korea STS 2016)

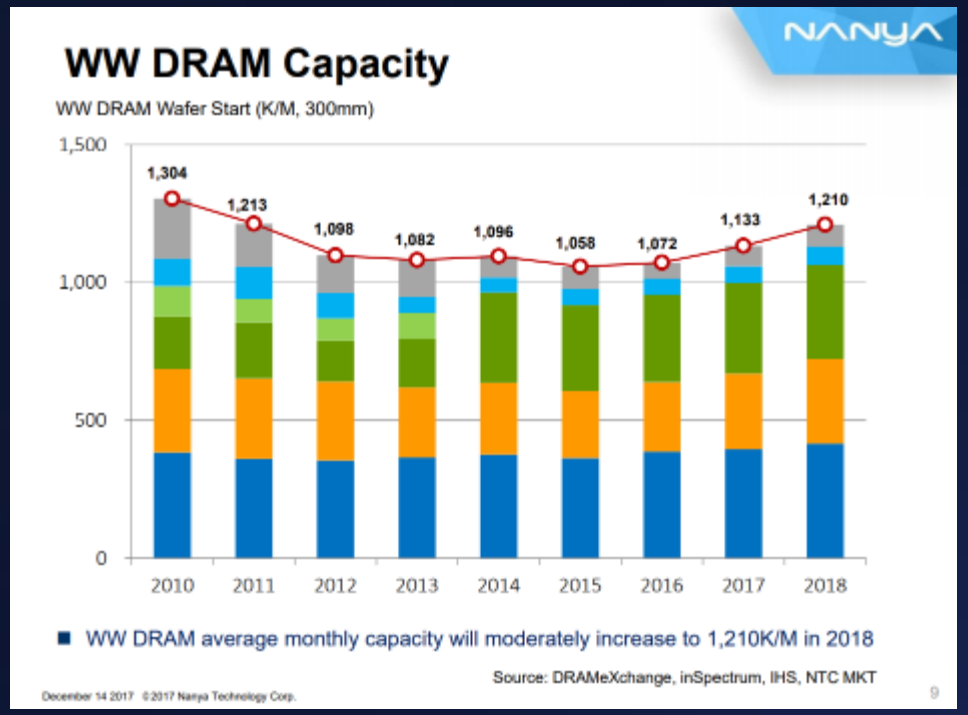
✓ Merit of device scaling is traded off by limited space of clean room floor

Red queen's race?

- Wafer fab spending and wafer capacity trend of world-wide DRAM



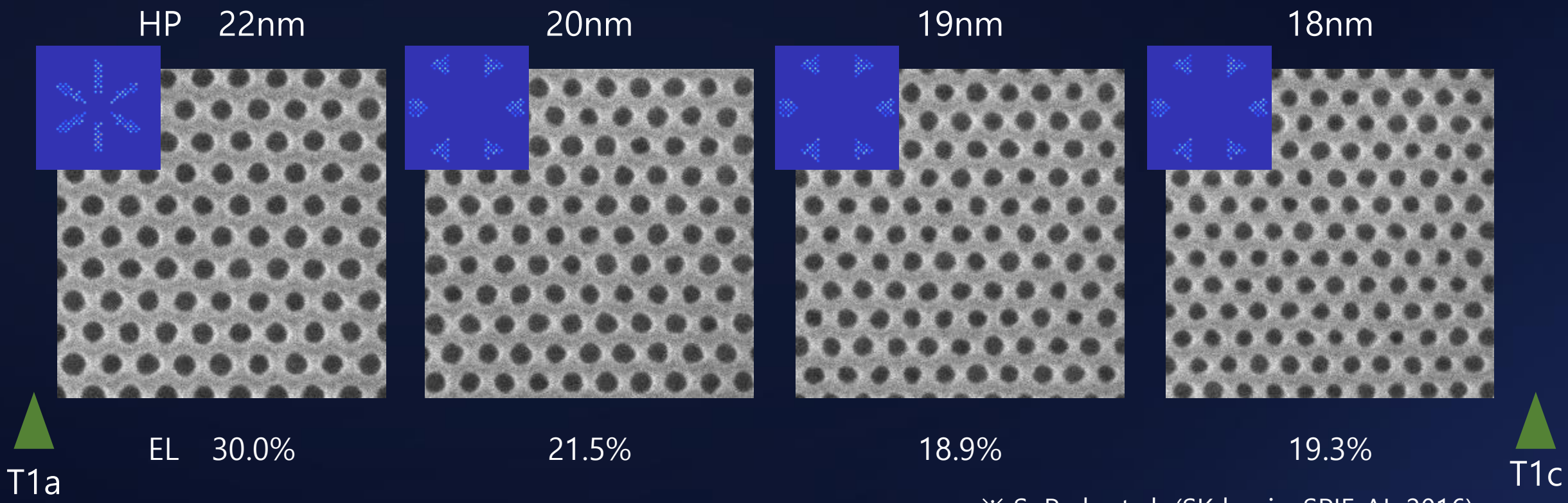
※ Source: IC insights



※ Presentation to analysts and investors by Nanya, 2017

✓ It's barely maintaining a status quo in wafer capacity with huge investment and expenditure on new fab building and equipment installation

Resolution of EUV

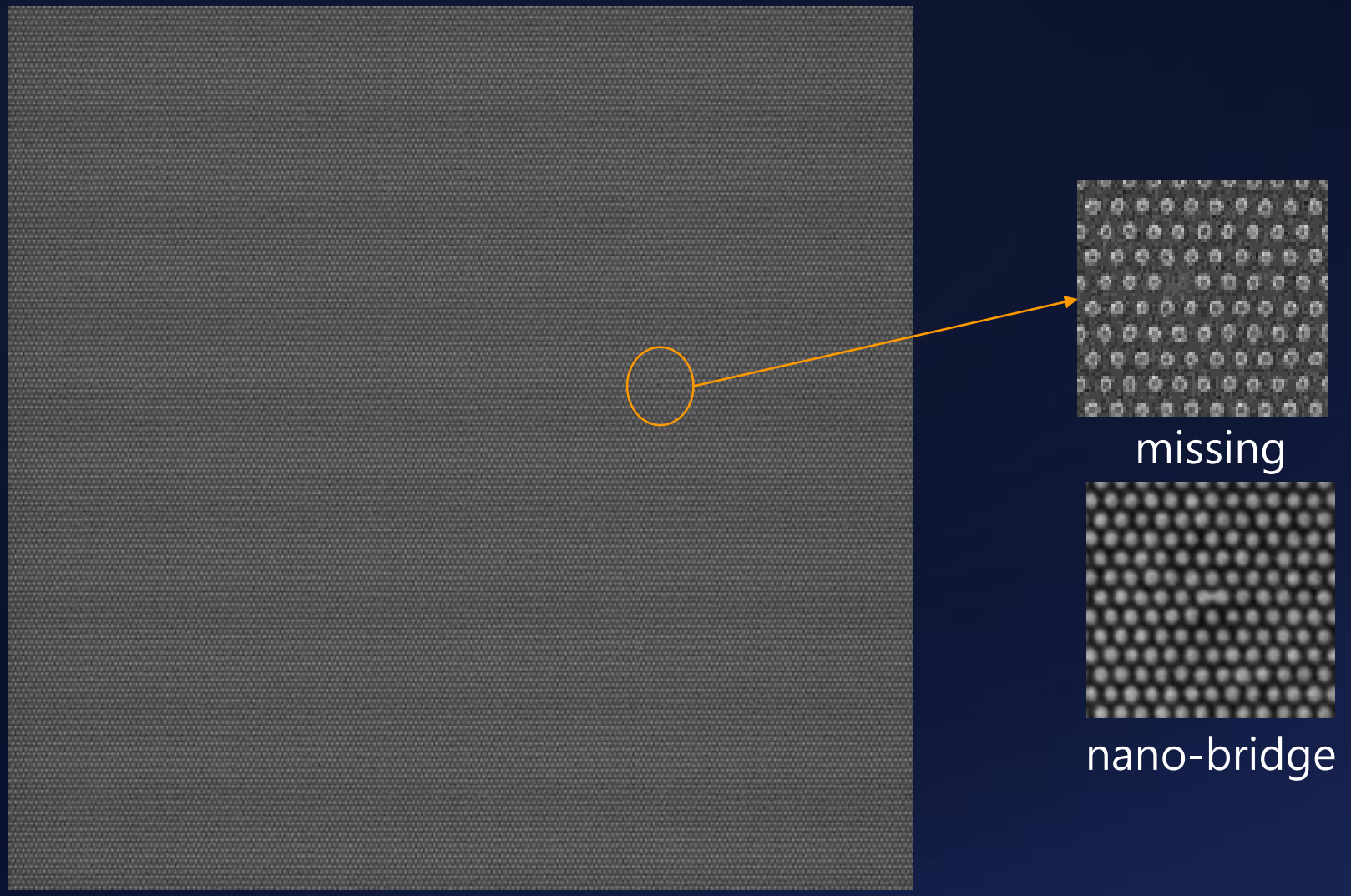


※ S. Park et.al. (SK hynix, SPIE AL 2016)

✓ EUV resolution is not limited by process window… already in 2016, 0.33NA EUV could resolve arrayed holes down to below 18nm without sophisticated optimization of illumination and mask condition

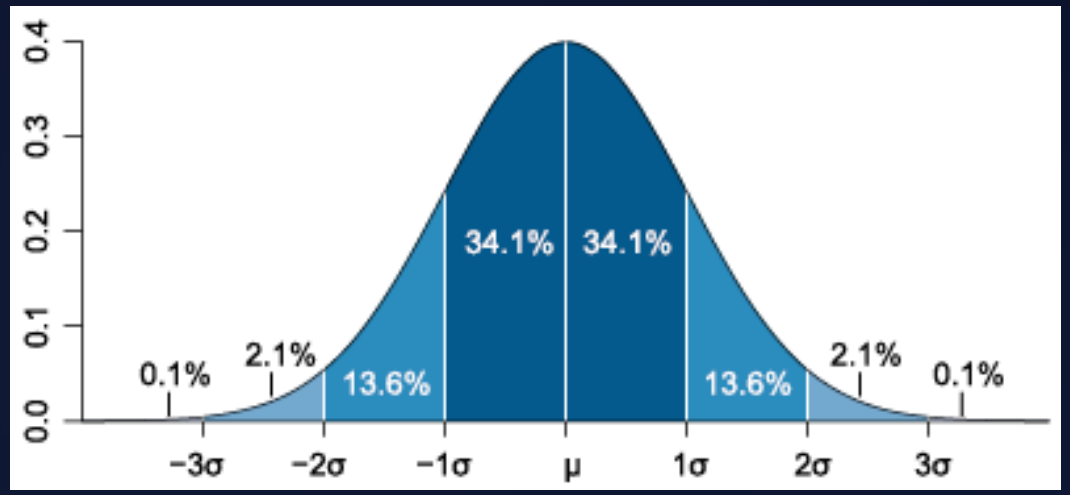
It's not that simple to make a 16 Billion bits

✓ $16x10^9$ holes or dots in a single chip and thousands of chips on a wafer



✓ 32 cells outside of ±6σ range is natural

It's before stochastics



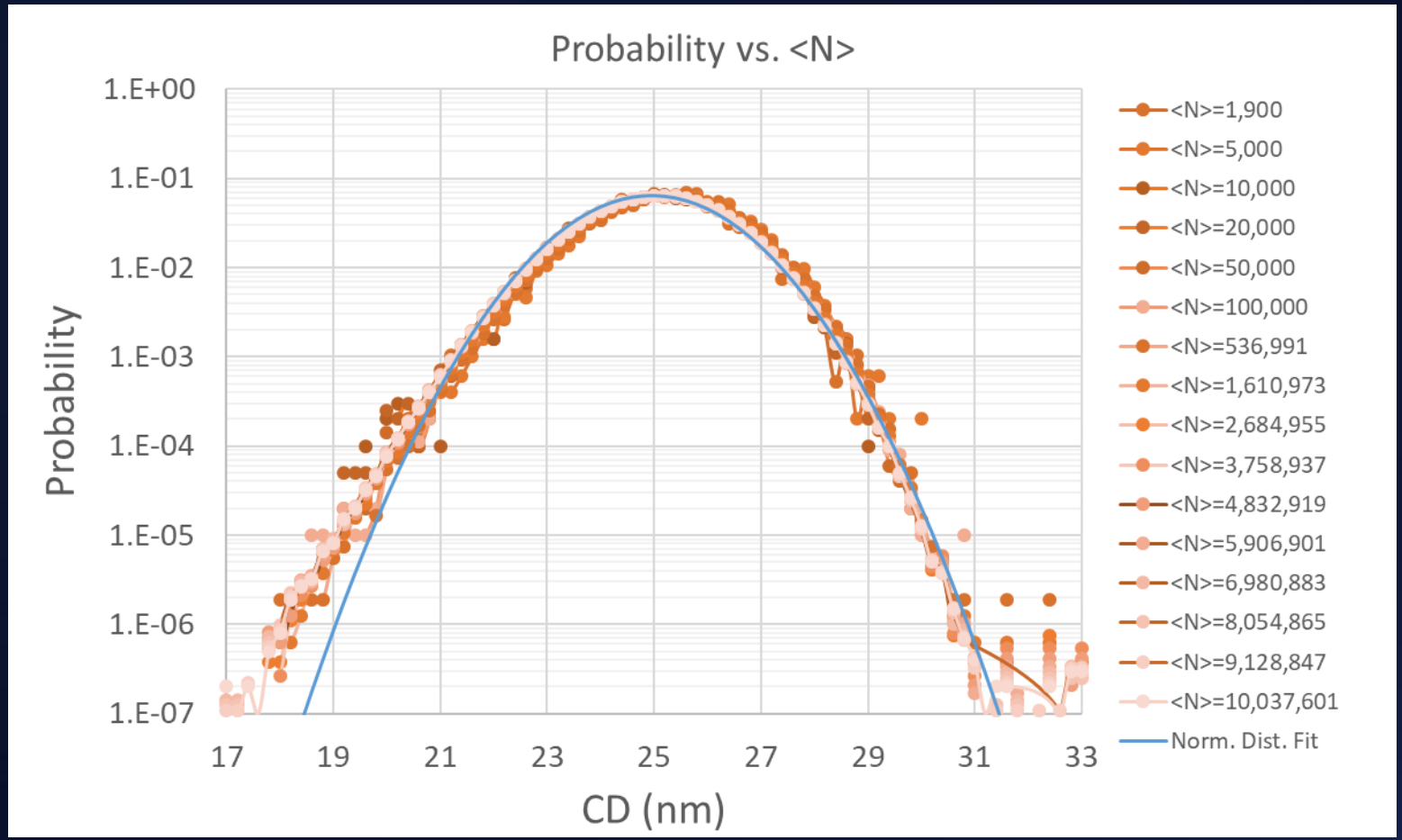
	in	out	Outlier in 16G chip
±1σ	0.682689492	0.317310507	5.44×10^9
±2σ	0.954499736	0.045500263	7.80×10^8
±3σ	0.997300204	0.002699796	4.64×10^7
±4σ	0.999936657	0.000063342	1.09×10^6
±5σ	0.999999426	0.000000573	9,948
±6σ	0.999999998	0.000000002	32

✓ Reminded that Gaussian distribution is also called a Normal distribution

No Normal distribution in real world

- Measured CD distribution along with number of measurements

※ Courtesy of Inhwan Lee(SK hynix)



- ✓ Asymmetric tail distribution come from nonlinear dose behavior but outliers are just rare event characteristics with certain contribution from measurement
- ✓ Control of CD distribution and uniformity in the end

Number of photons can be counted at EUV

6.7 photons/nm^2 @ 10mJ/cm^2

※ Note) $E = h\nu = h\frac{c}{\lambda}$

h=6.63x10^{-34} J·s
c=3.0x10^8 m/s

Photon shot noise or stochastics

Poisson distribution

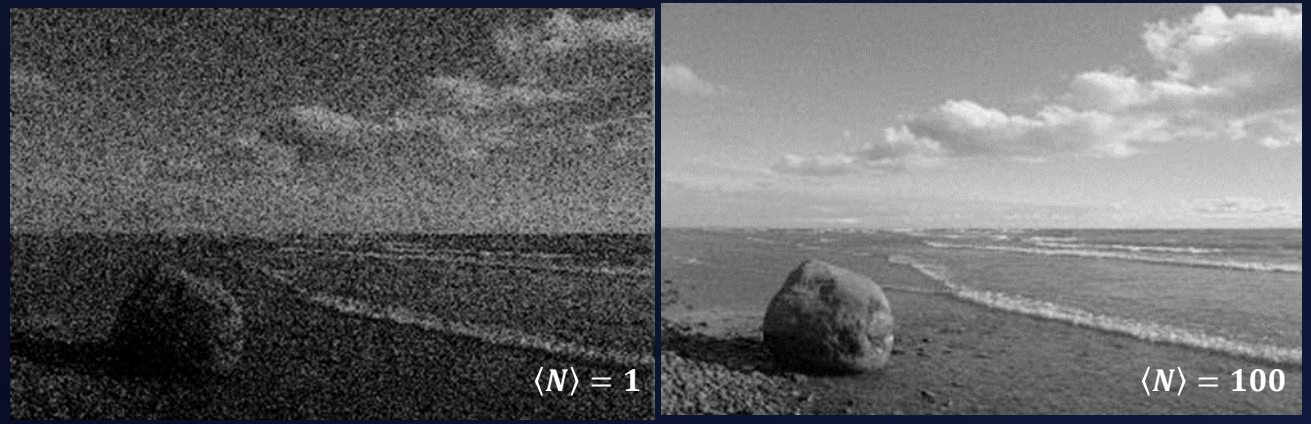
From Wikipedia, the free encyclopedia

In probability theory and statistics, the **Poisson distribution** (/ˈpwɑːsɒn/; French pronunciation: [pwasɔ̃]), named after French mathematician Siméon Denis Poisson, is a discrete probability distribution that expresses the probability of a given number of events occurring in a fixed interval of time or space if these events occur with a known constant mean rate and independently of the time since the last event.[1] The

When expectation value of countable event(ex., number of photons) is N, Standard deviation is $N^{1/2}$

$$\frac{\sigma}{mean} = \frac{1}{\sqrt{N}}$$

Images by shot noise



⟨N⟩ : average number of photons per pixel

▶ 1σ base

# of photons 100 → 100 ±10 (±10%)

10,000 → 10,000±100 (±1%)

※ https://en.wikipedia.org/wiki/Shot_noise#/media/File:Photon-noise.jpg

Consequence: Local CD variation vs. Dose

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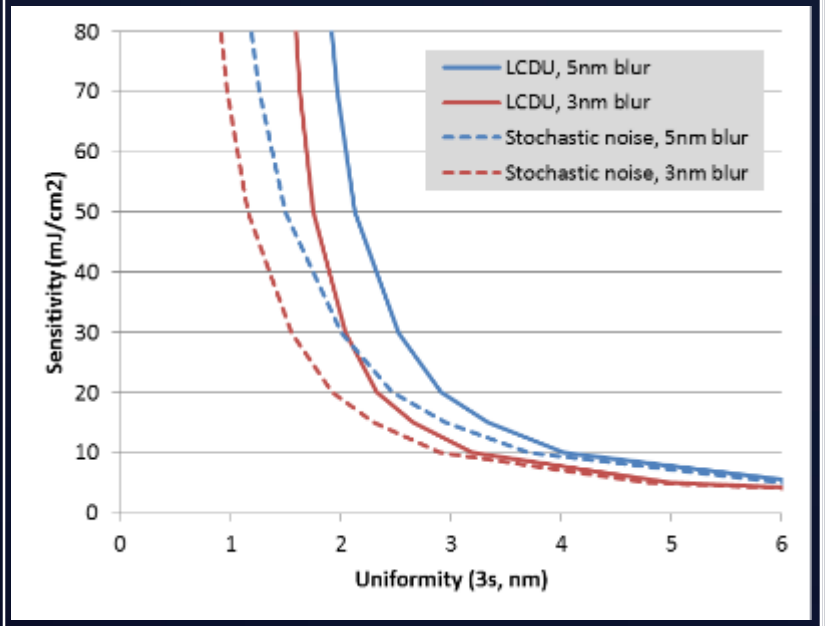
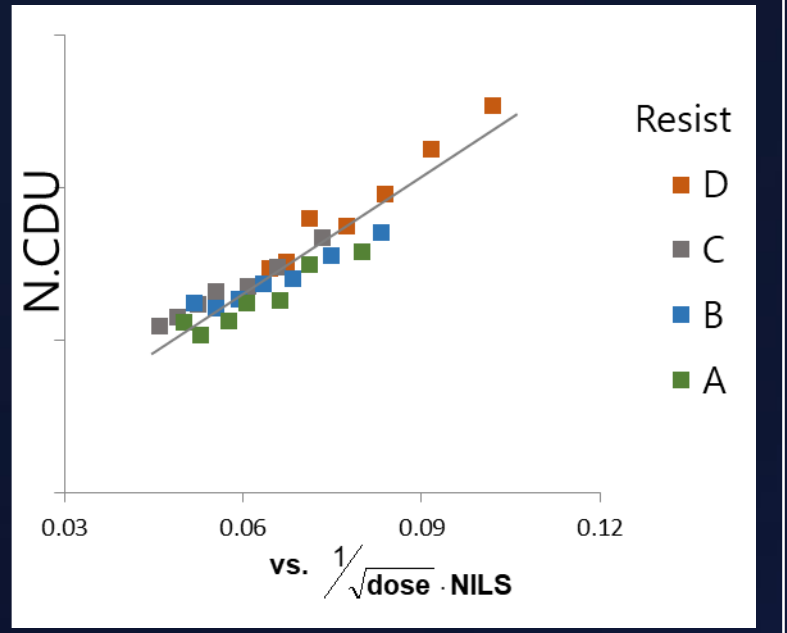
SPIE AL 2015
C. Ahn et.al. (ASML, SK hynix)



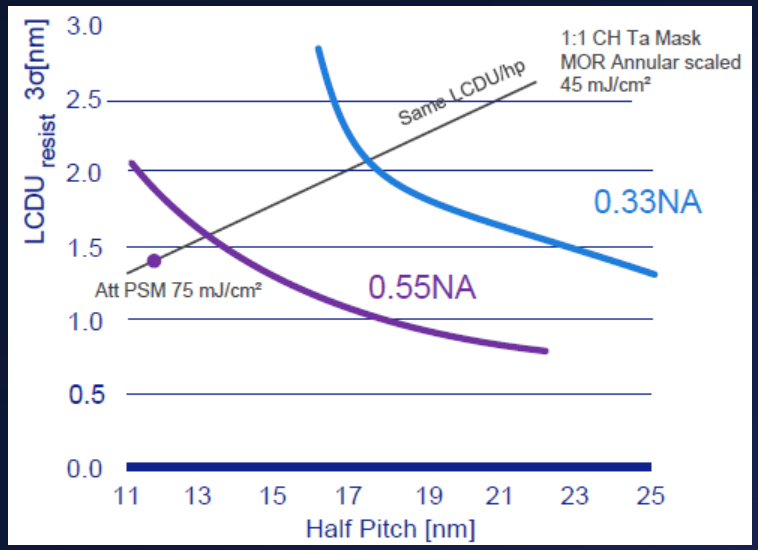
$$\sigma^2_{stochastic} \approx \left(\frac{2}{bILS}\right)^2 \left[1 + \frac{1}{2}\left(\frac{\partial \ln L'}{\partial \vec{\rho}} \cdot \vec{\beta}\right)^2\right] \frac{1}{\gamma \langle N \rangle}$$

SPIE AL 2016
S. Park et.al.(SK hynix)



$$LCDU \propto \frac{1}{\sqrt{dose} \cdot NILS}$$

EUVL workshop 2020
Jan van Schoot (ASML)



$$LCDU\ [3\sigma, nm] = 3 \cdot \sqrt{\frac{h\nu}{f \cdot \alpha \cdot Area}} \cdot \sqrt{\frac{1}{D_0}} \cdot \frac{2}{ILS}$$

✓ Inverse relationship of Dose, NILS and CDU

Consequence in value of lithography?

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Value of scaling through EUV

※ T. You et.al. (SK hynix, Semi Korea STS 2021)

Number of bits

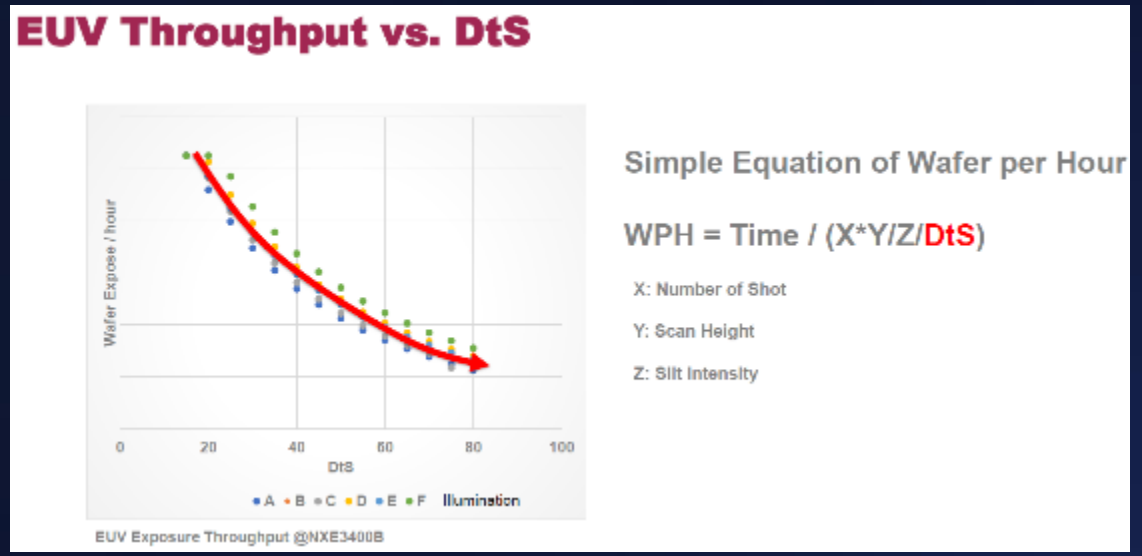
∝ Throughput x bits on wafer

↑ ~ $Dose^{-1}$ ↑ ~ $1/pitch^2$

~ $pitch^2$ x $NILS^2$

∝ **$NILS^2$**

$$LCDU\ [3\sigma, nm] = 3 \cdot \sqrt{\frac{h\nu}{f \cdot \alpha \cdot Area}} \cdot \sqrt{\frac{1}{D_0}} \cdot \frac{2}{ILS}$$

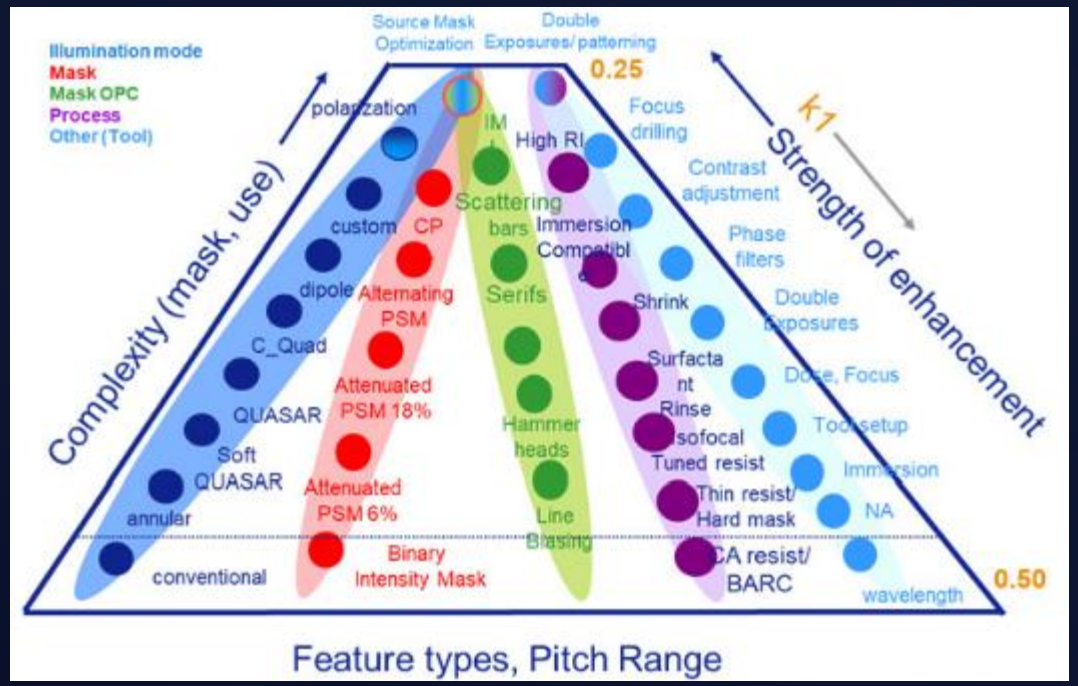


✓ Dead END for EUV?

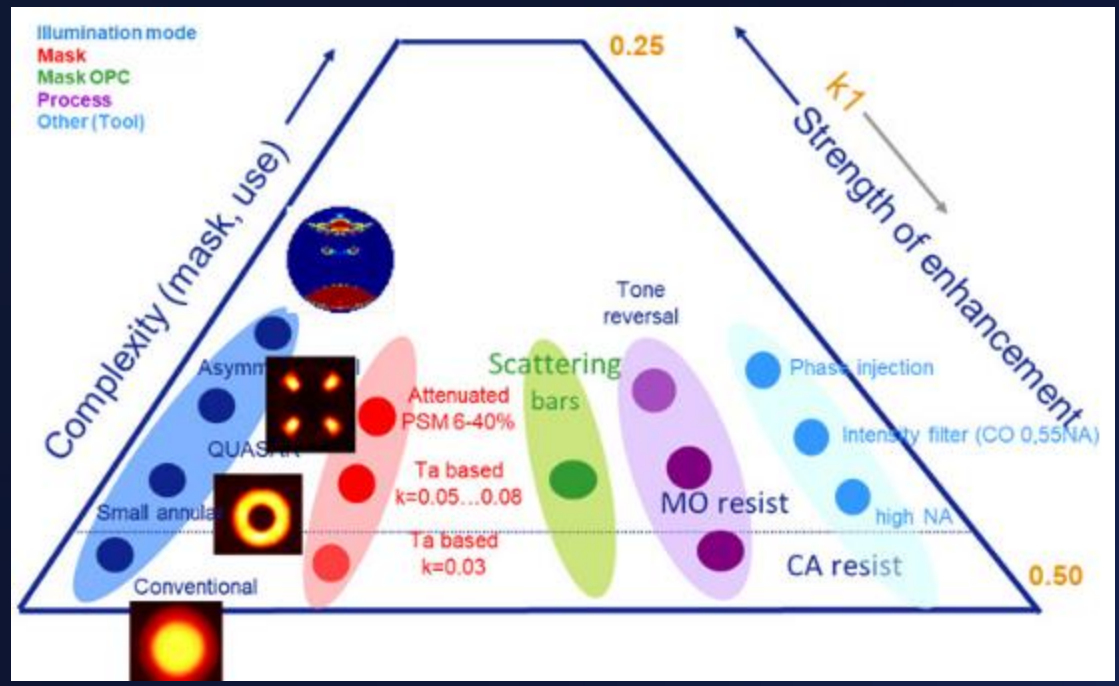
It has been our destiny, only we have not realized this way …

And we have to do what we've done

- ArFi hindsight



- EUV foresight

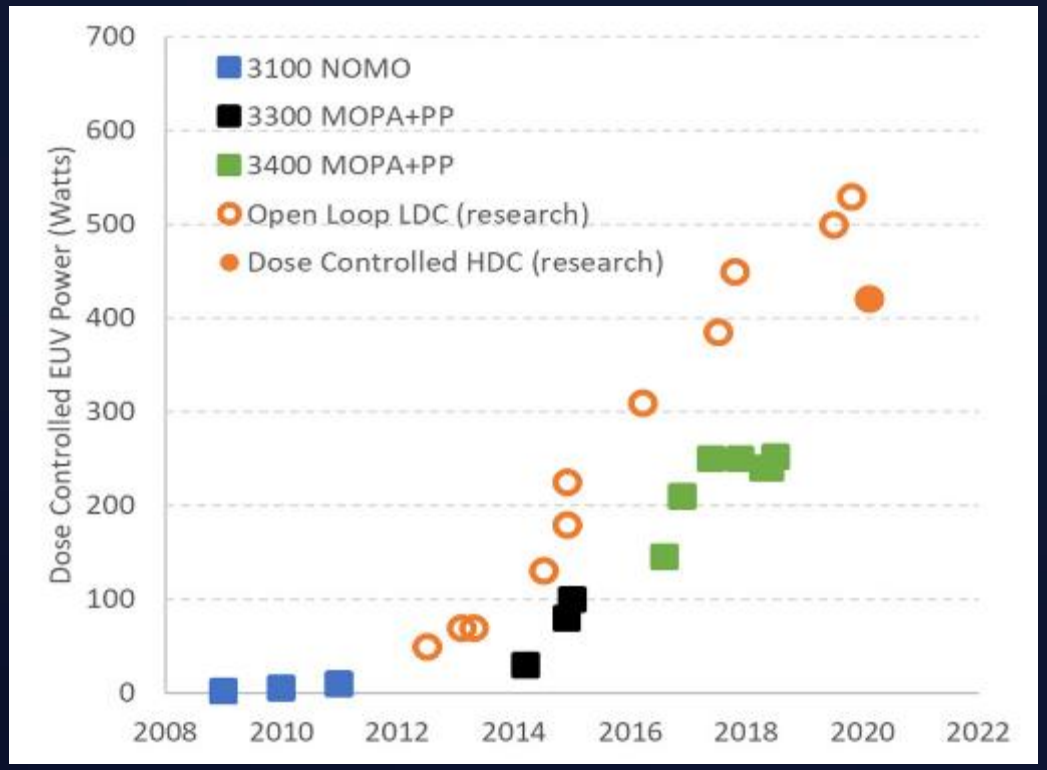


※ Jo Finders(ASML, SPIE AL 2021)

✓ Various technologies in every front have contributed to enhance resolution capability of immersion and it's time for EUV now

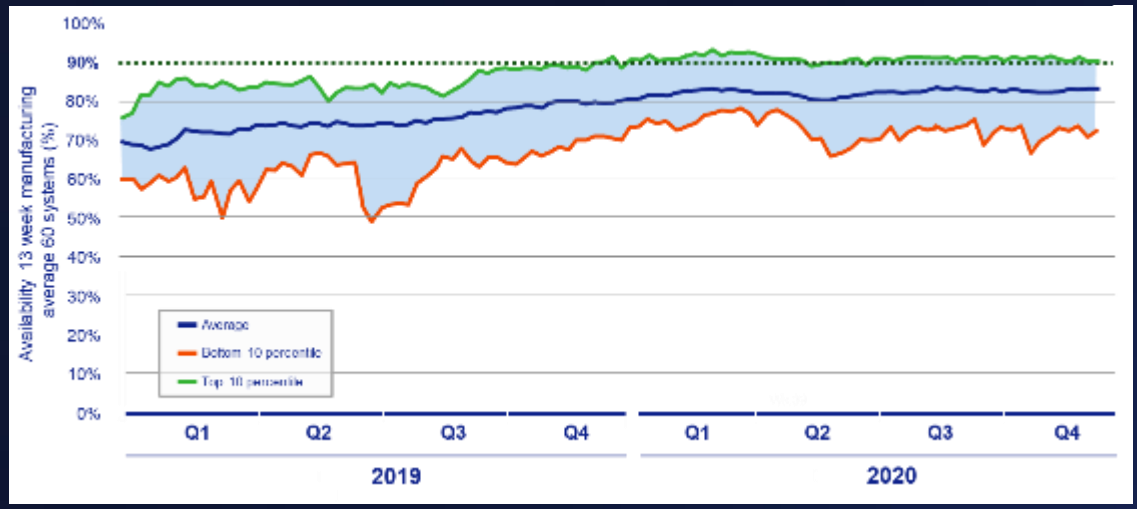
Increasing power and availability are prerequisite

- Progress of EUV source power



※ Jos Benschop(ASML, SPIE AL 2021)

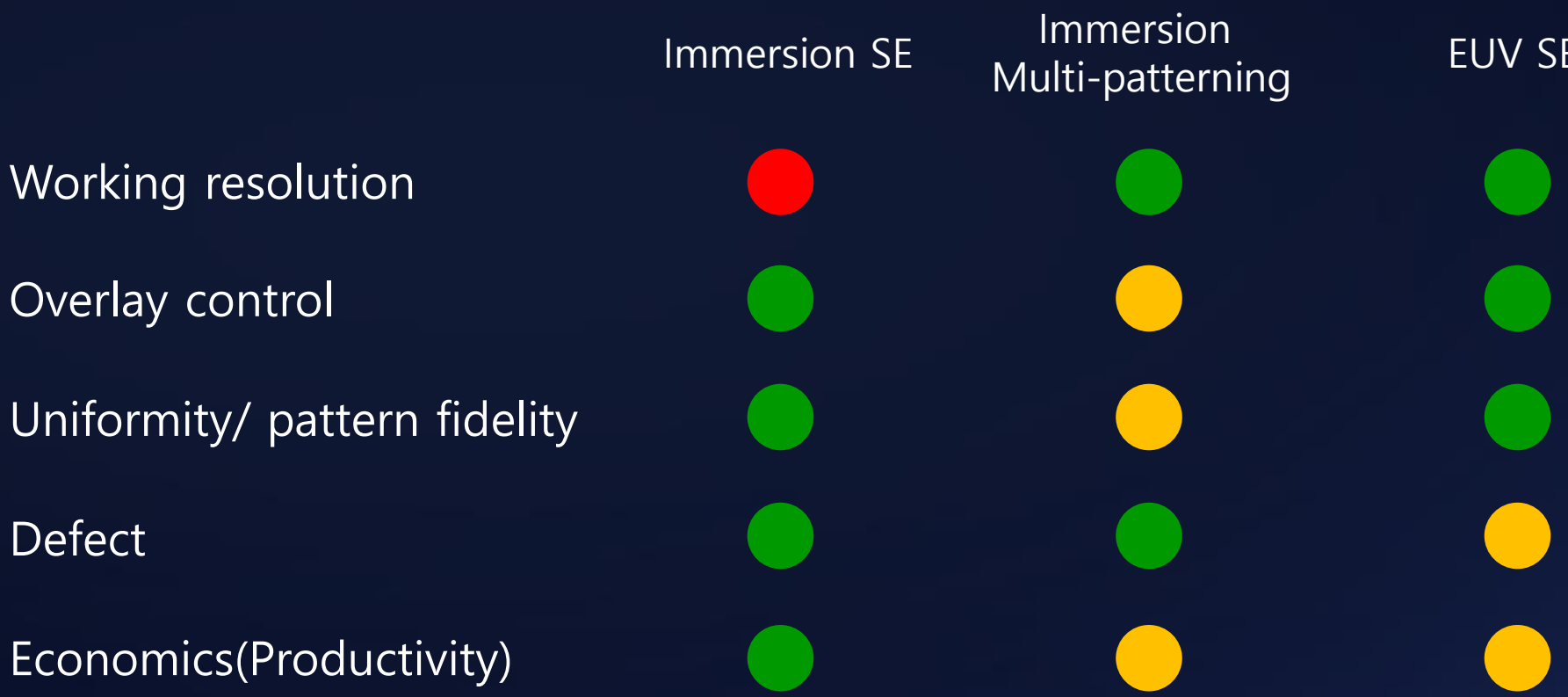
- Progress of machine availability



※ Eric Verhoeven(ASML, SPIE AL 2021)

✓ Increasing wafer level EUV intensity faster than the rise in cost, plus, improvement in machine availability for HVM are the necessary

Is EUV a Good Lithography?



- ✓ EUV lithography can't be as good as ArF immersion!
- ✓ Ultimate optimization and customized utilization are necessary!

SK Hynix's historical involvement on EUV

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>14 years of engagement and 3 gen. scanners on site operation experience

'07, joined IMEC

2011, NXE3100

2014, NXE3300B

'18, NXE3400B

'21, NXE3400C

Finally on the start-line

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SK hynix announces the Completion of M16 Plant Construction

SK hynix NEWSROOM

~~~ What's more special about M16 is its introduction of the extreme ultraviolet (EUV) lithography equipment for the first time in SK hynix. The company plans to grow this plant as a next-generation growth source based on the cutting-edge infrastructure. It plans to produce 1a nm DRAM products from the second half of this year by utilizing the EUV equipment. Also, the company plans to increase the utilization of this equipment in the future to further strengthen the technology leadership in the advanced processing of semiconductor memories. ~~~
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Summary

Status

Sky after Typhoon
(http://festival.jangheung.go.kr/)

New EUV fab open and preparation under-going to start T1a production from 2nd half of this year

Challenges

Google images

EUV technology will not be as perfect as immersion lithography for DRAM (Stochastics, pellicle-less, tool…), *only limitless sophistication can makes it better lithography solution*

Conclusion

Canopus taken from ISS

SK Hynix plan to use EUV to overcome scaling challenges and continue to develop sub 10nm DRAM onwards

http://spaceflight.nasa.gov/gallery/images/station/crew-6/hires/iss006e28068.jpg

Thank you for attention!

Acknowledgements
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Sunyoung Koo
Taewoo Jung
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