EUV Mask Substrate Readiness For Sub 10 nm HP Nodes

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Outline

- EUV mask substrate requirements
  - Flatness
  - Roughness
  - Defects
- EUV mask substrate manufacturing
- Progress in EUV mask substrate in Applied Materials
- EUV mask substrates for sub 10 nm nodes
Substrate Requirements: Critical Parameters

- Multiple parameters should be controlled both in the front and back surface.
- All parameters are interdependent within each surface and between both surfaces.

Ideal substrate

Real substrate

Front side

Backside

Bow

Wedge

Local slope angle

Wedge angle

Flatness (FS)

Roughness (FS)

Bow

Roughness (BS)

Flatness (BS)
Substrate Flatness & Bow Contribution to Overlay Errors

- Mask bow and flatness can lead to IPD and OPD errors some of which can NOT be corrected by scanner
- Substrate is the main contributor to mask flatness and bow
Substrate Roughness Contribution to EUV Mask

- EUV reflectivity is reducing by increasing substrate surface roughness
- Line edge roughness is increasing by increasing replicated substrate surface roughness
- Defect count is increasing by increasing substrate roughness due to dependency of inspection tools to the surface roughness
Manufacturing of EUV Mask Blank Substrates

Each polishing step removes and creates subsurface damage. Remaining subsurface damage results in pit and scratches.

Advances in CMP/Polishing technologies, T.K. Doi, et al.
Substrate defectivity has improved by 3 orders of magnitude within a year without sacrificing substrate flatness (i.e. PV)
Substrate flatness has improved by ~6x within a year without sacrificing defectivity
Progress In ULE Substrate Flatness Reduction (Advanced Polishing)

- Advanced polishing techniques were used to achieve PV=16 nm
Progress In ULE Substrate Bow Reduction In Applied Materials

- Substrate bow was reduced by 25x within a year without sacrificing defectivity
EUV mask substrates for sub 10 nm HP nodes

- Increase in EUV source power (>250 W)
  - More heat should be dissipated by substrate
  - Depending on cooling rate higher $T_{zc}$ LTEM material may required
- Substrate roughness
  - Should be about 50 pm (HFSR) for inspection and defectivity
- Substrate flatness
  - PV < 10 nm may required to reduce overlay errors
- Substrate defectivity
  - Critical defect size of defect on substrate may not change
Printable substrate defects

- All pits defects on substrate with (depth < 2nm, width < 20 nm) were smoothed by deposition process.
- Only defects with (depth >0.6nm, width >30 nm) on multilayer were detected by actinic inspection at the time.

Substrate defects with (height/depth > 2nm and FWHM > 20 nm) (SEVD=12 nm) are critical.

12 nm on mask → 3 nm on wafer.
Summary & conclusions

- EUV mask blank performance is determined by many interdependent parameters of substrate that need to be optimized simultaneously
  - Surface flatness (PV, local slope and bow)
  - Surface roughness
  - Defectivity
  - Multiple polishing tools and cleaning tools and process need to be optimized.

- As multilayer deposition processes are becoming efficient, substrate yield will be the main driver for the price of the EUV blanks

- The higher power EUV source and pellicles will generate more heat on substrate that require LTEM materials be optimized for higher temperature (Higher $T_{ZC}$)

- Applied Materials has demonstrated considerable improvement in substrate development within a year
  - Defectivity: 3 order of magnitude reduction $\rightarrow$ 6@ 34 nm
  - PV: 6x reductions $\rightarrow$ PV=52 nm (16 nm Adv. polishing)
  - Bow: 25x reduction $\rightarrow$ bow = 6 nm

Substrate development took > 10 years in industry