EUV patterning improvement toward high-volume manufacturing

2015 International Workshop on EUV Lithography

Tokyo Electron Kyushu Ltd. / SPE process dept.
Y. Kuwahara, K. Matsunaga, K. Nafus, S. Kawakami
imec
P. Foubert, A-M. Goethals
Introduction

• Extreme ultraviolet lithography (EUVL) technology is a promising candidate of semiconductor process for 18nm half pitch and beyond. It still requires fine resolution, uniform, smooth patterns and low defectivity, not only after lithography but also after the etch process.

• Tokyo Electron Limited and imec are continuously collaborating to develop manufacturing quality POR processes to EUV with CLEAN TRACK™ LITHIUS Pro™Z-EUV. We evaluated defectivity at post lithography and post etch process. New rinse material and application compatible with sub 18nm patterning is performed to prevent line pattern collapse on several resist materials, because rinse material compatibility with resist is concerned.
EUVL 32nm L/S Defects after Litho

Embedded Defect reduction is the Key Challenge

Target Defect

Yuhei Kuwahara/TEL – Philippe Foubert
/imec et. al, SPIE 2014

Defect Budget
SPIE2014

1. Coating related 74% (UL, EM, MB, Prt)
2. Collapse 25%

Coating related defects are still majority of the defectivity
Baseline Defectivity Result ADI&AEI

After etch inspection is much more sensitive, post etch defect reduction need to be addressed.
Coating related defect reduction is important to after etch defect reduction.
Coating Defect Reduction by New Technologies at TEL in-house

Before verification of pattern defect, executed preliminary test for coating defect reduction by new dispense system.

New Function can reduce blanket coating defect for several materials

Defect Inspection: KLA2900 (KLA-Tencor)

ACI defects

Protrusion

Dent

Embedded

Normalized Blanket Defect

- Protrusion
- Dent
- Embedded

Baseline | New  | Baseline | New
---|---|---|---
SiARC | 81% | EUV Resist-C | 71%

81%

71%
Root cause of AEI defects are investigated by using coating defect reduction technologies.
AEI Defect Reduction Result

- Defectivity is drastically improved by New Function, AEI defectivity is sensitive with coating defect.
- Micro bridge and Embedded defect reduction is main contributor.
Pattern Collapse Mitigation

σ = 6γcosθ/D × (h/W)^2

σ: The maximum stress which works to pattern collapse
γ: Surface tension of rinse
θ: Contact angle
h: Height of pattern
D: Space of pattern
W: Width of pattern
h/W: Aspect ratio


Approach to tackle this challenge
- Surface tension reduction by introducing a New ‘FIRM™ Material’

Check the resist compatibility below 20nm pattern
FIRM™ Rinse Material Evaluation
20nmHP of Resist-B

<table>
<thead>
<tr>
<th>Process window</th>
<th>DIW Rinse</th>
<th>Extreme™10</th>
<th>Extreme™ A</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>CD [nm]</th>
<th>Dose [mJ/cm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIW</td>
<td>17.6</td>
</tr>
<tr>
<td>Extreme™ 10</td>
<td>16.8</td>
</tr>
<tr>
<td>Extreme™ A</td>
<td>15.2</td>
</tr>
</tbody>
</table>

- No collapses
- Unavailable pattern (collapse, no resolution, melt)

※Extreme™ is a registered trademark of AZ Electronic Materials.

<table>
<thead>
<tr>
<th></th>
<th>smallest CD [nm]</th>
<th>△CD from DIW [nm]</th>
<th>LWR [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIW</td>
<td>17.6</td>
<td>-</td>
<td>7.1</td>
</tr>
<tr>
<td>Extreme™10</td>
<td>16.8</td>
<td>1.0</td>
<td>6.8</td>
</tr>
<tr>
<td>Extreme™ A</td>
<td><strong>15.2</strong></td>
<td>-0.2</td>
<td>7.2</td>
</tr>
</tbody>
</table>

✔ Extreme™ A has
- best smallest CD without pattern collapse.
- Smaller CD change from DIW process than Extreme™ 10

※Extreme™ is a registered trademark of AZ Electronic Materials.

- No collapses
- Unavailable pattern (collapse, no resolution, melt)
FIRM™ Rinse Material Resist Compatibility below 20nm Pattern

<table>
<thead>
<tr>
<th>Half pitch / Resist</th>
<th>DIW</th>
<th>Extreme™ 10</th>
<th>Extreme™ A</th>
</tr>
</thead>
<tbody>
<tr>
<td>HP 18nm / Resist-D</td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
<td><img src="image3" alt="Image" /></td>
</tr>
<tr>
<td>Dose</td>
<td><img src="image4" alt="Image" /></td>
<td><img src="image5" alt="Image" /></td>
<td><img src="image6" alt="Image" /></td>
</tr>
<tr>
<td>Focus</td>
<td><img src="image7" alt="Image" /></td>
<td><img src="image8" alt="Image" /></td>
<td><img src="image9" alt="Image" /></td>
</tr>
<tr>
<td>HP 17nm / Resist-E</td>
<td><img src="image10" alt="Image" /></td>
<td><img src="image11" alt="Image" /></td>
<td><img src="image12" alt="Image" /></td>
</tr>
<tr>
<td>Dose</td>
<td><img src="image13" alt="Image" /></td>
<td><img src="image14" alt="Image" /></td>
<td><img src="image15" alt="Image" /></td>
</tr>
<tr>
<td>Focus</td>
<td><img src="image16" alt="Image" /></td>
<td><img src="image17" alt="Image" /></td>
<td><img src="image18" alt="Image" /></td>
</tr>
<tr>
<td>Available:8</td>
<td>Available:9</td>
<td>Available: 8</td>
<td></td>
</tr>
</tbody>
</table>

- **Yellow**: No collapses
- **Brown**: Unavailable pattern (collapse, no resolution, melt)

** ✓ Extreme™ A shows pattern collapse mitigation for**
- Below 20nm pattern
- Several resist materials

<table>
<thead>
<tr>
<th></th>
<th>smallest CD [nm]</th>
<th>△CD [nm]</th>
<th>LWR [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HP 18nm / Resist-D</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIW</td>
<td>16.7</td>
<td>-</td>
<td>6.9</td>
</tr>
<tr>
<td>Extreme™ 10</td>
<td>16.0</td>
<td>1.7</td>
<td>6.4</td>
</tr>
<tr>
<td>Extreme™ A</td>
<td><strong>14.9</strong></td>
<td>0.4</td>
<td>6.9</td>
</tr>
<tr>
<td><strong>HP 17nm / Resist-E</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DIW</td>
<td>16.2</td>
<td>-</td>
<td>8.5</td>
</tr>
<tr>
<td>Extreme™ 10</td>
<td>17.6</td>
<td>1.2</td>
<td>8.0</td>
</tr>
<tr>
<td>Extreme™ A</td>
<td><strong>15.2</strong></td>
<td>0.1</td>
<td>8.2</td>
</tr>
</tbody>
</table>
18nm HP Process Window and X-section SEM with Resist-E

**18nm HP Process Window**

<table>
<thead>
<tr>
<th>CD±5%</th>
<th>DIW Rinse</th>
<th>Extreme™10</th>
<th>Extreme™A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max EL</td>
<td>4.3%</td>
<td>8.9%</td>
<td>6.9%</td>
</tr>
<tr>
<td>Max DoF</td>
<td>80nm</td>
<td>80nm</td>
<td><strong>280nm</strong></td>
</tr>
<tr>
<td>Dose to Size</td>
<td>36.3(mJ/cm²)</td>
<td>38.3(mJ/cm²)</td>
<td>36.2(mJ/cm²)</td>
</tr>
</tbody>
</table>

**18nm HP X-section**

<table>
<thead>
<tr>
<th>DIW Rinse</th>
<th>Extreme™10</th>
<th>Extreme™A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height: 24-29nm</td>
<td>Height: 21-28nm</td>
<td>Height: 25-31nm</td>
</tr>
</tbody>
</table>

- Extreme™ A achieved
  - greater process window than Extreme10
  - no significant impact to pattern profile and thickness
L16nm P36nm with Extreme™A and Resist-E

FIRM Extreme™10

Total 532 images/wafer

FIRM Extreme™A

Collapse

Ave. CD 16.4nm
3sigma: 1.6nm

Ave. CD 16.6nm
3sigma: 0.7nm

0% Standing Ratio 100%

Pattern collapse is completely mitigated by FIRM Extreme™A on 16nm line pattern.
Conclusion

✓ Defect reduction is key for the EUV manufacturing, especially post etch defectivity.
✓ Post Etch defectivity is reduced 85% by using New Function.
✓ Pattern collapse is one of the critical issue of the EUV lithography.
✓ FIRM Extreme™A has demonstrated greater pattern collapse mitigation and process window enhancement on even below 20nm HP pattern.
✓ In addition, FIRM Extreme™A has great compatibility with several imec POR materials.
Acknowledgement

• The authors would like to extend their appreciation to
  – Tokyo Electron Kyushu Ltd. SPE Process Technology department
  – Tokyo Electron Europe Ltd. service team
  – Tokyo Electron Miyagi Ltd. Product engineering