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EUV patterning improvement toward high-volume manufacturing

2015 International Workshop on EUV Lithography

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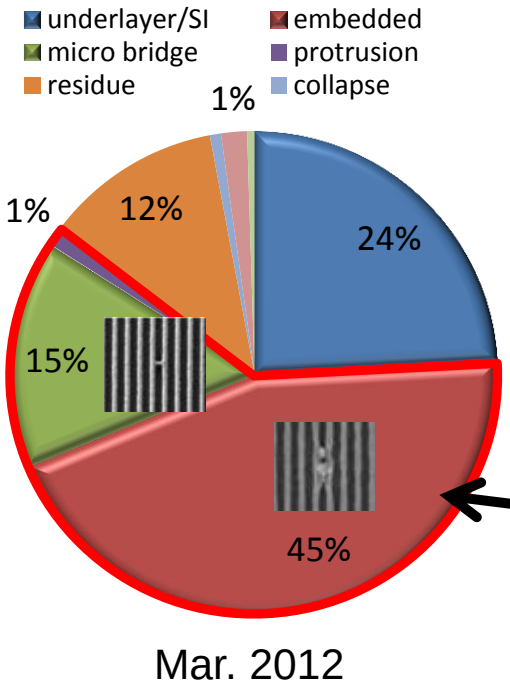
Introduction

- Extreme ultraviolet lithography (EUVL) technology is a promising candidate of semiconductor process for 18nm half pitch and beyond.
  It still requires fine resolution, uniform, smooth patterns and low defectivity, not only after lithography but also after the etch process.

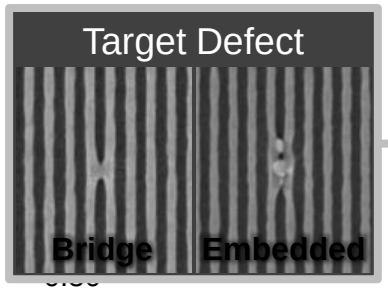
- Tokyo Electron Limited and imec are continuously collaborating to develop manufacturing quality POR processes to EUV with CLEAN TRACK™ LITHIUS Pro™Z-EUV.
  We evaluated defectivity at post lithography and post etch process.
  New rinse material and application compatible with sub 18nm patterning is performed to prevent line pattern collapse on several resist materials, because rinse material compatibility with resist is concerned.

EUVL 32nm L/S Defects after Litho

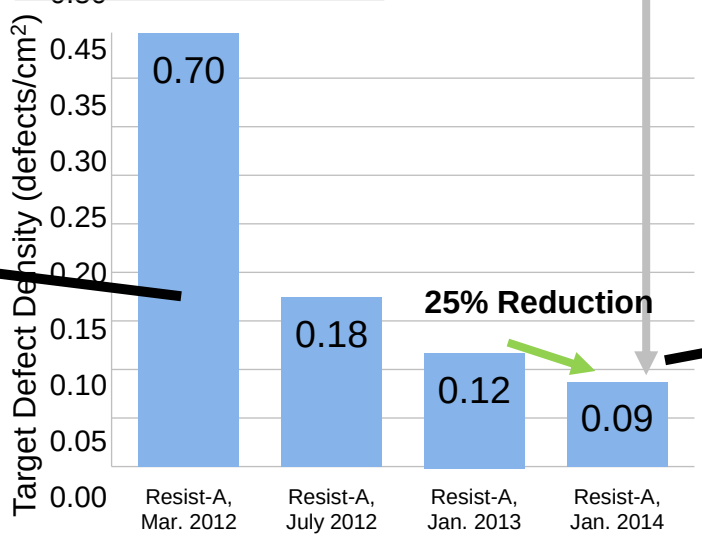
Embedded Defect reduction is the Key Challenge

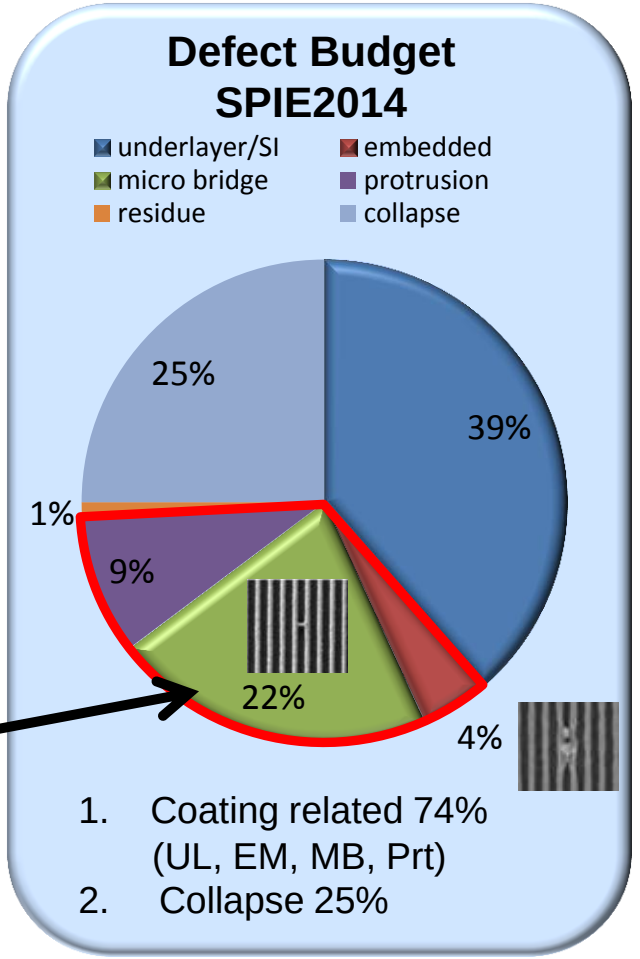


Mar. 2012



Yuhei Kuwahara/TEL – Philippe Foubert
/imec et. al, SPIE 2014

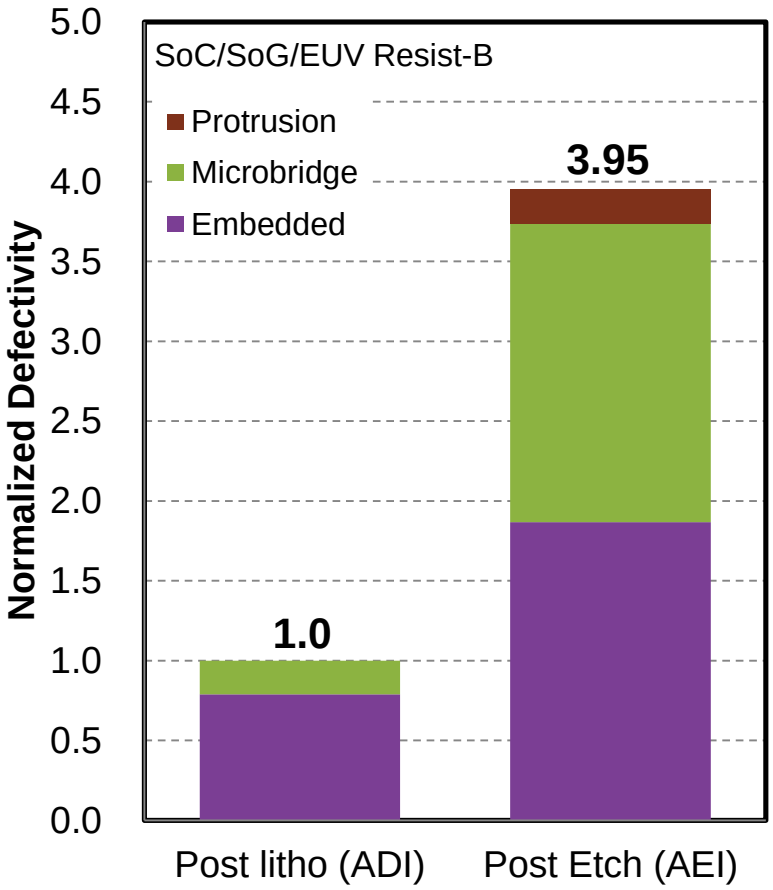




1. Coating related 74% (UL, EM, MB, Prt)
2. Collapse 25%

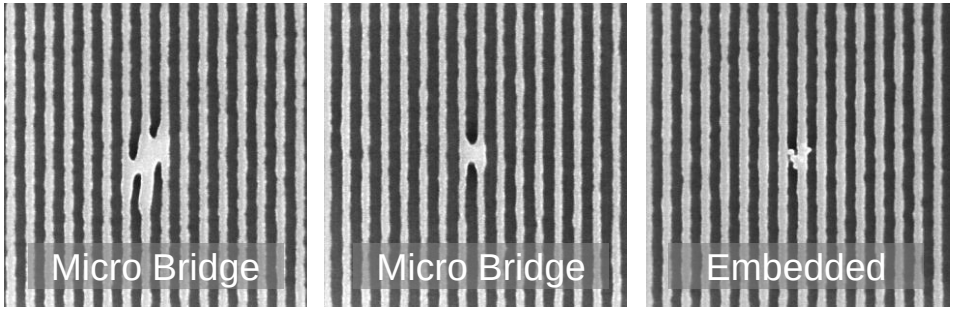
✓ **Coating related defects are still majority of the defectivity**

Baseline Defectivity Result ADI&AEI

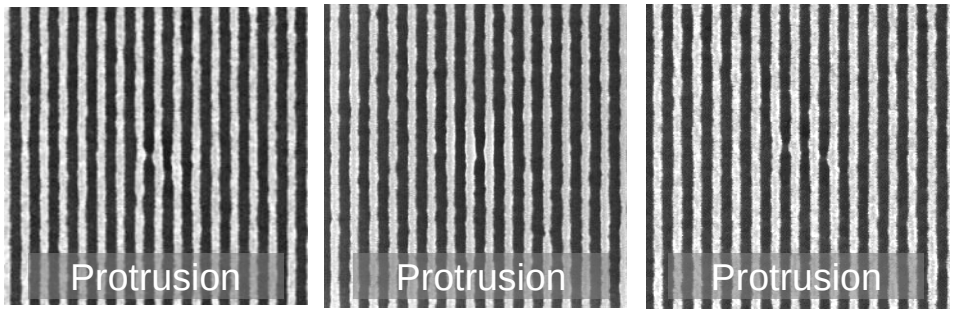


AEI Defect Images

ADI&AEI Common Defect



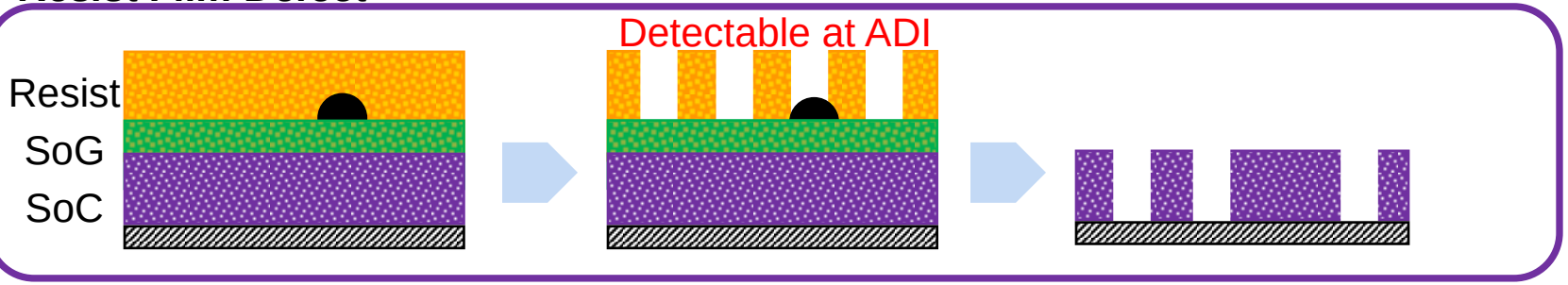
AEI Specific Defect



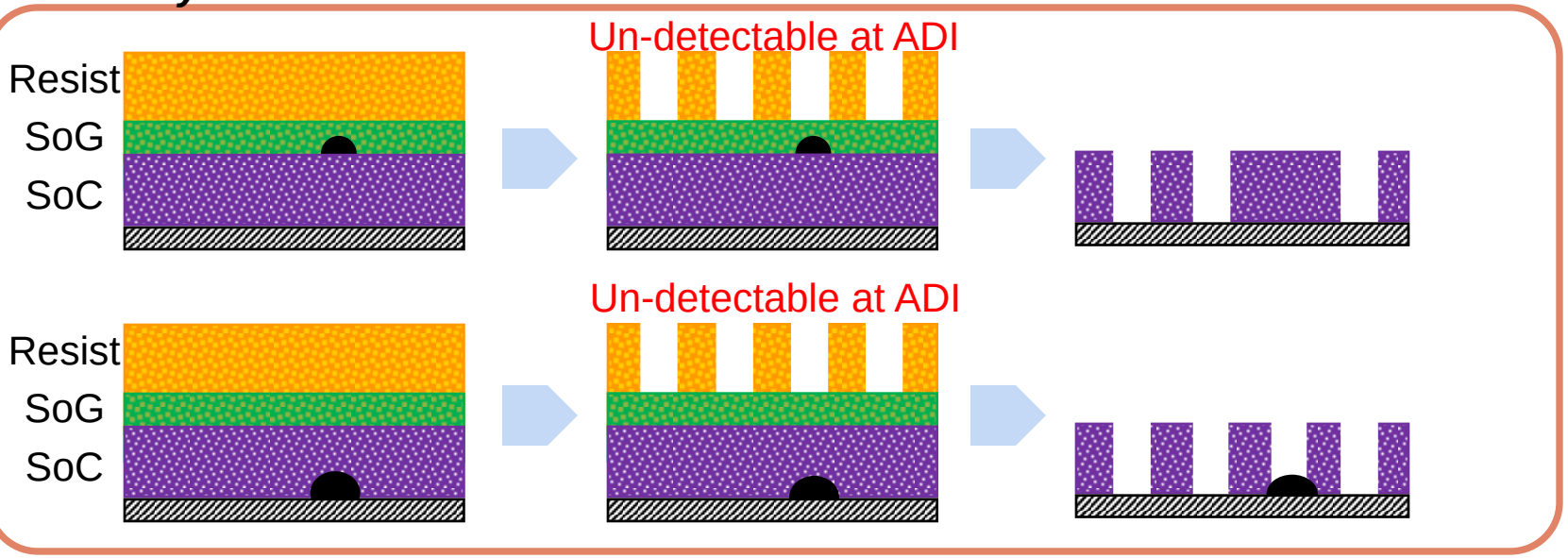
✓ **After etch inspection is much more sensitive, post etch defect reduction need to be addressed.**

After Etch Defect Model

Resist Film Defect



Under Layer Film Defect



✓ **Coating related defect reduction is important to after etch defect reduction**

Coating Defect Reduction by New Technologies at TEL in-house

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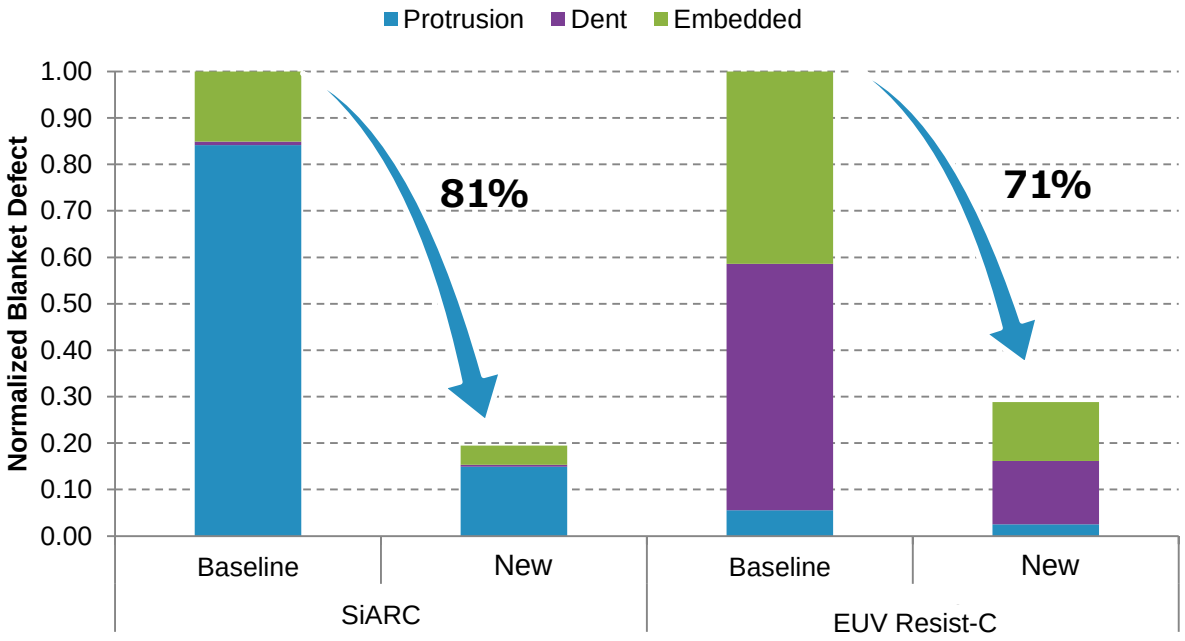
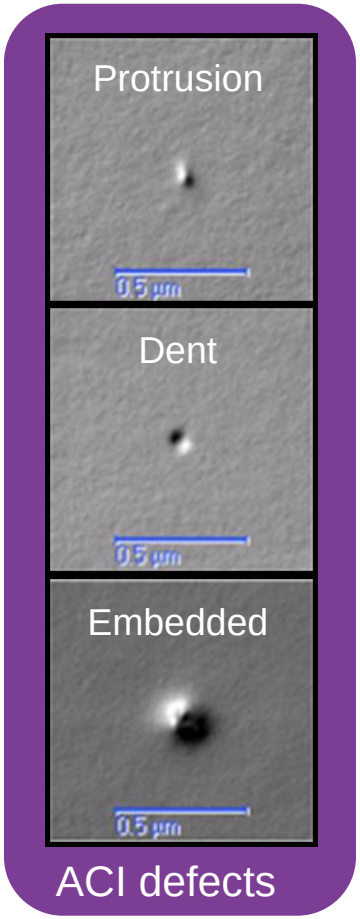
Defect Inspection：KLA2900 (KLA-Tencor)

Before verification of pattern defect , executed preliminary test for coating defect reduction by new dispense system.

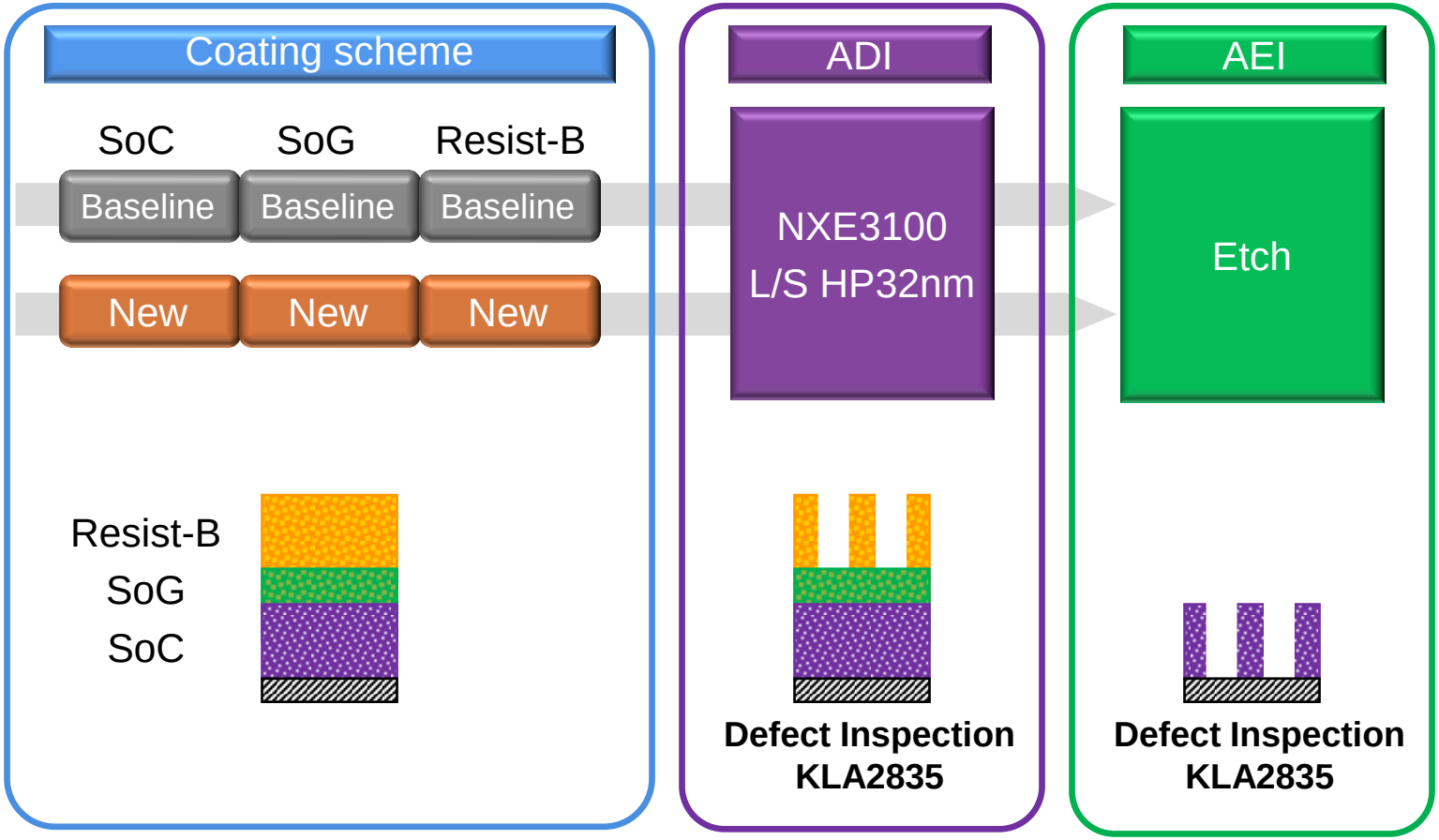




✓ **New Function can reduce blanket coating defect for several materials**

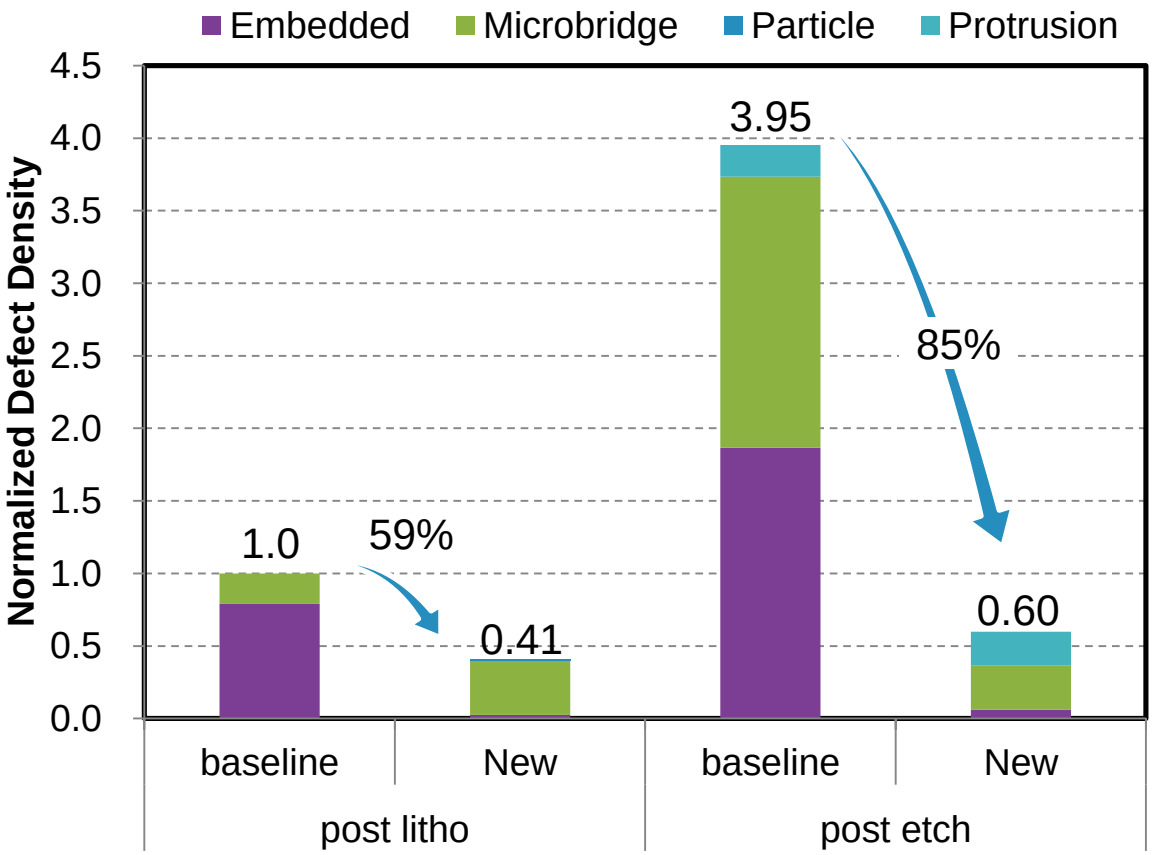
Evaluation of AEI Defect Reduction

Experiment Flow

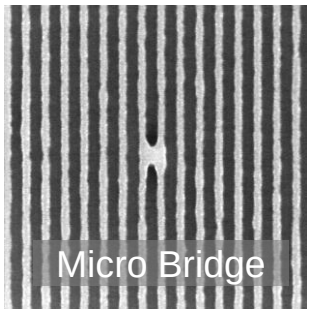


✓ **Root cause of AEI defects are investigated by using coating defect reduction technologies.**

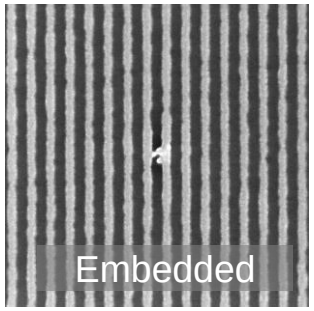
AEI Defect Reduction Result



AEI Defect Images



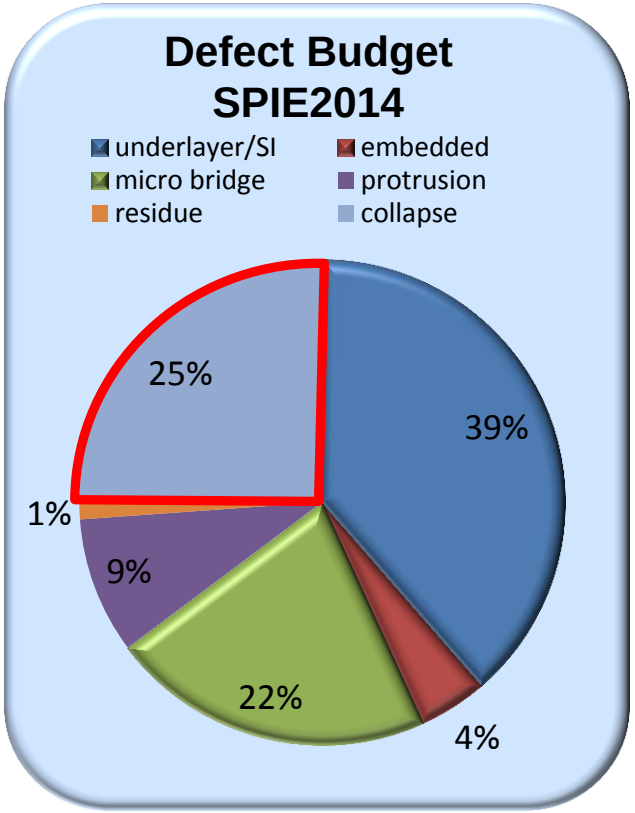
Total 97% Reduction

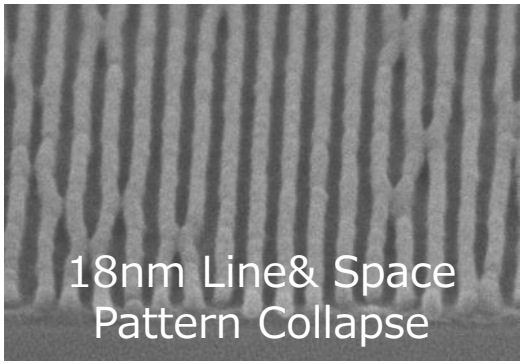


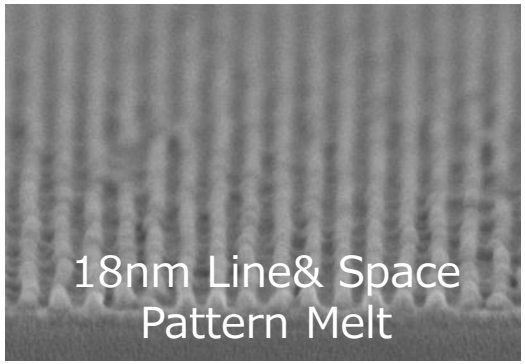
Total 84% Reduction

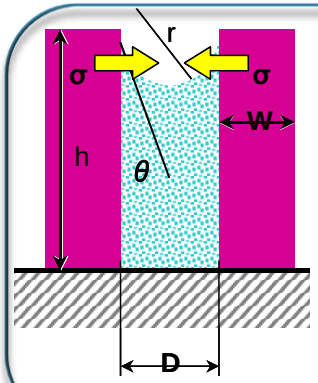
- ✓ Defectivity is drastically improved by New Function, AEI defectivity is sensitive with coating defect.
- ✓ Micro bridge and Embedded defect reduction is main contributor.

Pattern Collapse Mitigation









$$\sigma = 6\gamma\cos\theta / D \times (h/W)^2$$

σ ; The maximum stress which works to pattern

γ ; Surface tension of rinse θ ; Contact angle

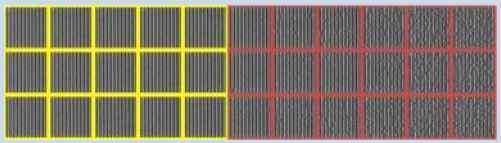
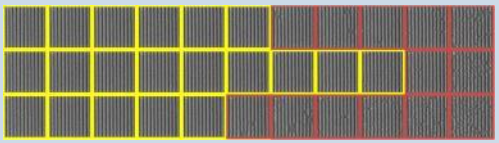
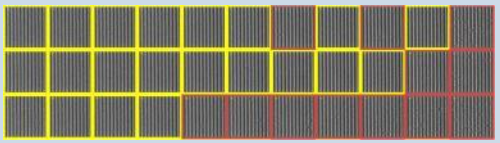
h ; Height of pattern D ; Space of pattern

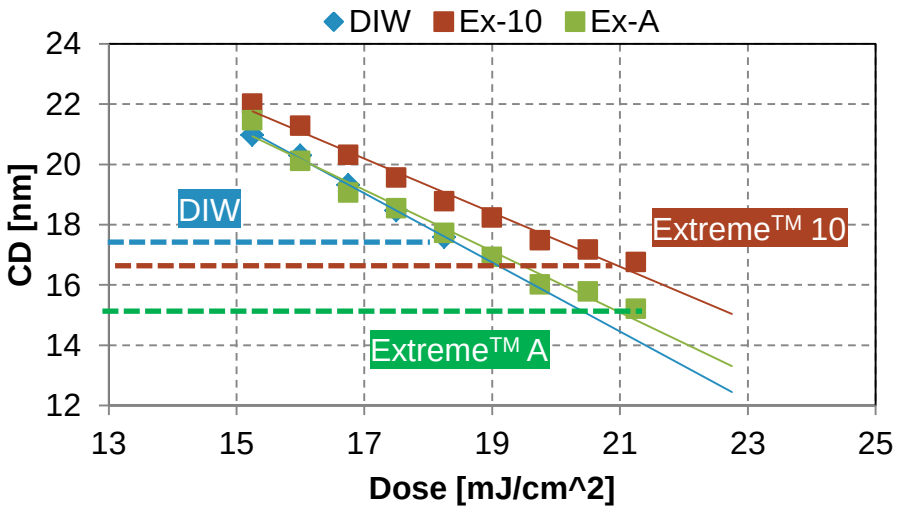
W ; Width of pattern h/W ; Aspect ratio

N. Namatsu *et. al., Appl.. Phys. Lett.* 66(20), pp.2655-2657, (1995)

- ✓ Approach to tackle this challenge
  - Surface tension reduction by introducing a New 'FIRM™ Material'
- ✓ Check the resist compatibility below 20nm pattern

FIRM™ Rinse Material Evaluation 20nmHP of Resist-B

	DIW Rinse	Extreme™10	Extreme™ A
Process window (Dose →, Focus ↓)			
	Available:15	Available:20	Available: 21



No collapses

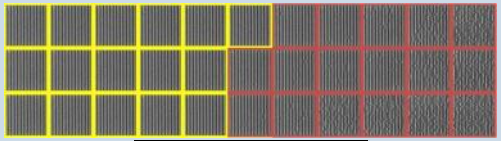
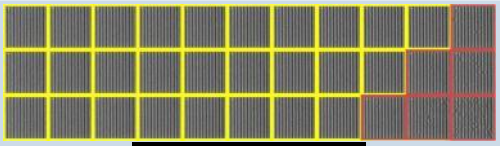
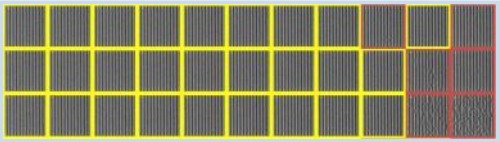
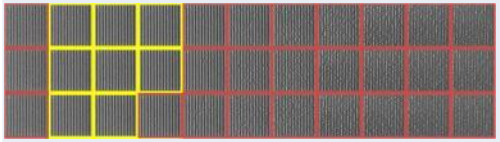
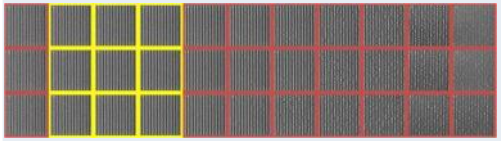
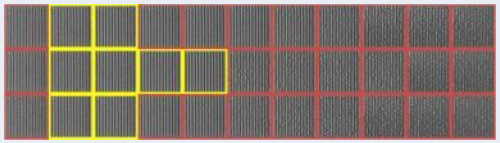
Unavailable pattern (collapse, no resolution, melt)

※Extreme™ is a registered trademark of AZ Electronic Materials.

	smallest CD [nm]	⊿CD from DIW [nm]	LWR [nm]
DIW	17.6	-	7.1
Extreme™10	16.8	1.0	6.8
Extreme™ A	**15.2**	-0.2	7.2

- ✓ Extreme™ A has
  - best smallest CD without pattern collapse.
  - Smaller CD change from DIW process than Extreme™ 10

FIRM™ Rinse Material Resist Compatibility below 20nm Pattern

Half pitch / Resist	DIW	Extreme™10	Extreme™ A
HP 18nm / Resist -D (Dose →, Focus ↓)	 Available:16	 Available:27	 Available: 27
HP 17nm / Resist-E (Dose →, Focus ↓)	 Available:8	 Available:9	 Available: 8

No collapses

Unavailable pattern (collapse, no resolution, melt)

- ✓ Extreme™ A shows pattern collapse mitigation for
  - Below 20nm pattern
  - Several resist materials

		smallest CD [nm]	⊿CD [nm]	LWR [nm]
HP 18nm / Resist-D	DIW	16.7	-	6.9
	Extreme™10	16.0	1.7	6.4
	Extreme™ A	**14.9**	0.4	6.9
HP 17nm / Resist-E	DIW	16.2	-	8.5
	Extreme™10	17.6	1.2	8.0
	Extreme™ A	**15.2**	0.1	8.2

18nm HP Process Window and X-section SEM with Resist-E

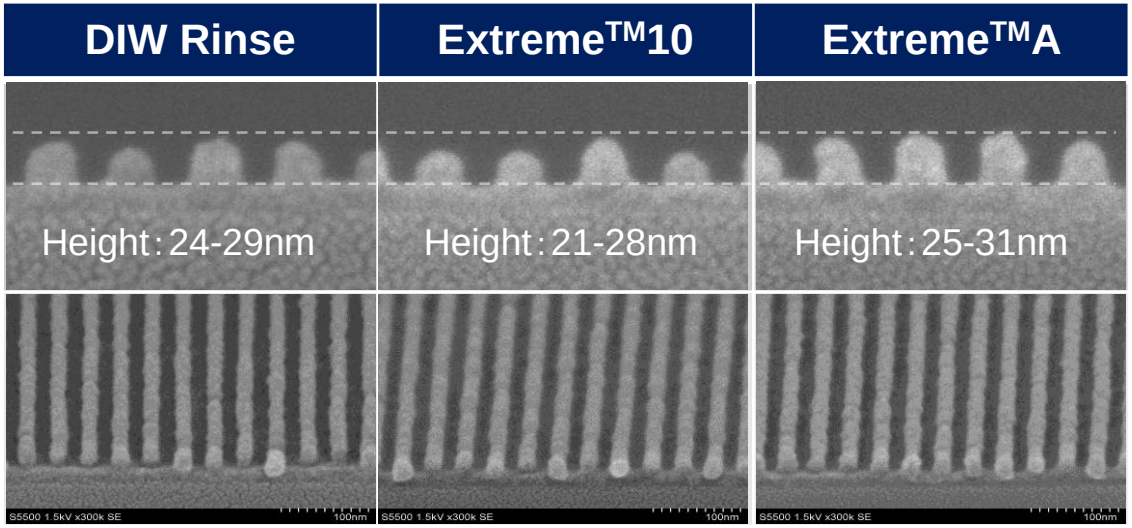
Merck KGaA Darmstadt · Germany

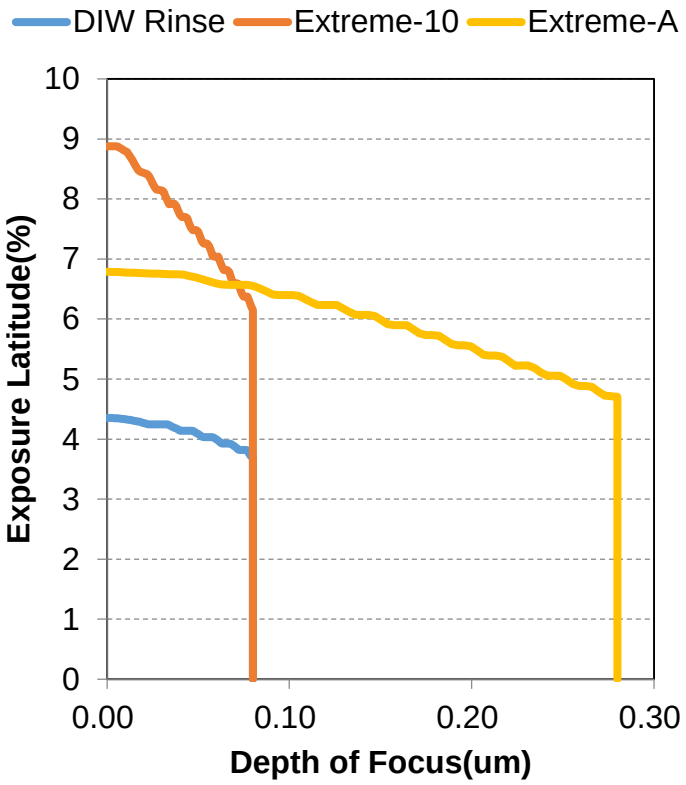
imec

18nm HP Process Window

CD±5%	DIW Rinse	Extreme™10	Extreme™A
Max EL	4.3%	8.9%	6.9%
Max DoF	80nm	80nm	**280nm**
Dose to Size	36.3(mJ/cm²)	38.3(mJ/cm²)	36.2(mJ/cm²)

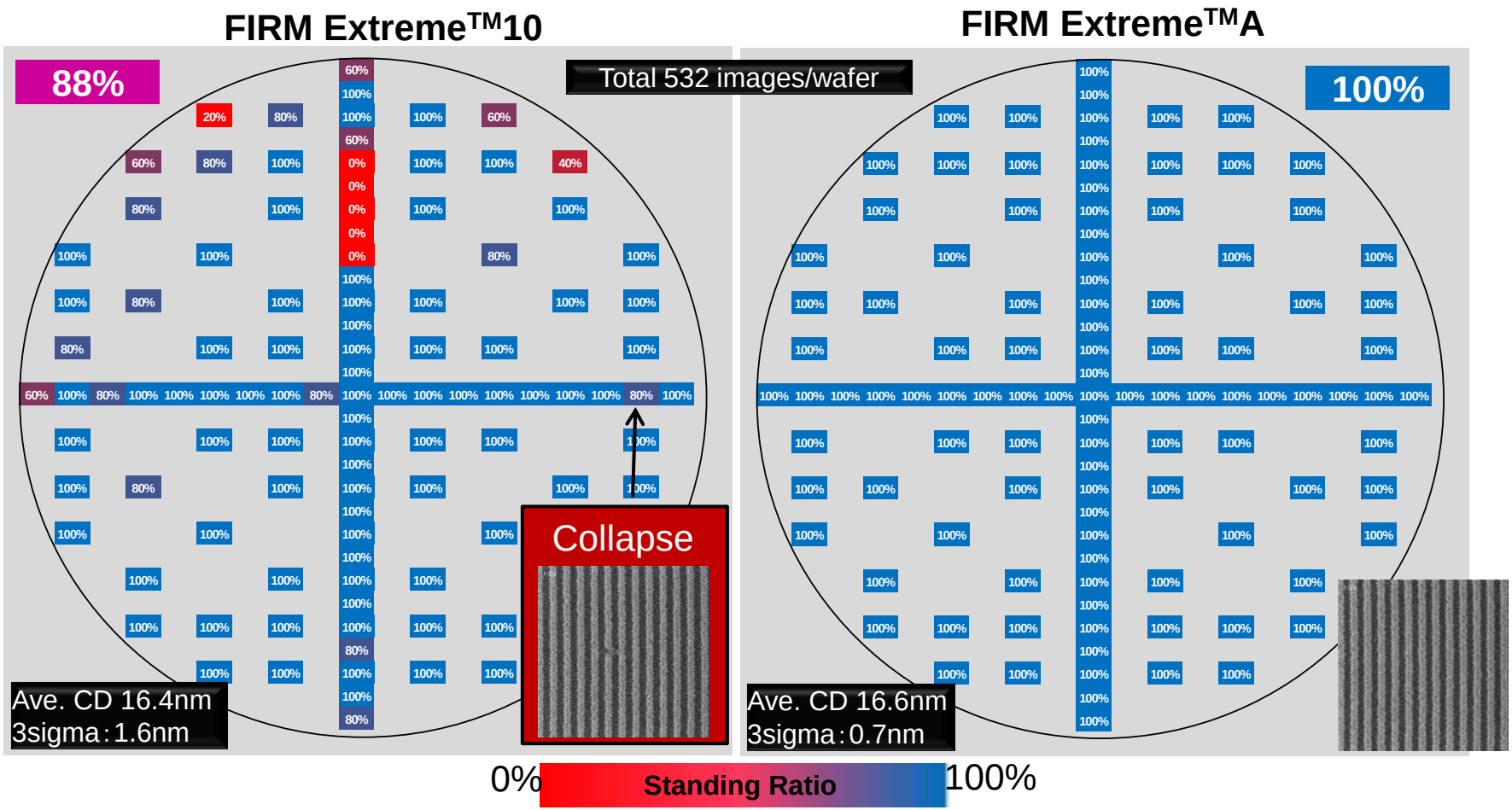
18nm HP X-section





- ✓ **Extreme™ A achieved**
  - **greater process window than Extreme10**
  - **no significant impact to pattern profile and thickness**

L16nm P36nm with Extreme™A and Resist-E



✓ **Pattern collapse is completely mitigated by FIRM Extreme™A on 16nm line pattern.**

Conclusion

- ✓ Defect reduction is key for the EUV manufacturing, especially post etch defectivity.
- ✓ Post Etch defectivity is reduced 85% by using New Function.
- ✓ Pattern collapse is one of the critical issue of the EUV lithography.
- ✓ FIRM Extreme™A has demonstrated greater pattern collapse mitigation and process window enhancement on even below 20nm HP pattern.
- ✓ In addition, FIRM Extreme™A has great compatibility with several imec POR materials.

Acknowledgement

- **The authors would like to extend their appreciation to**
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  - Tokyo Electron Europe Ltd. service team
  - Tokyo Electron Miyagi Ltd. Product engineering