Challenges of EUV lithography for HVM

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TOSHIBA Corporation
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  - 1\textsuperscript{st} step for HVM; requirements for pilot production
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- Summary
Introduction

Lithography Challenges
Lithography history

Resolution or CD

- Contact exposure
- G-line WL: 436nm
- i-line 365nm
- High NA & shorter WL
  - KrF 248nm
  - ArF 193nm
  - ArF imm 193nm
- Chemically amplified resist
- Excimer laser
- RET/ OPC
- Computational lithography
- Double/multiple Patterning

Resolution = k1 \frac{\lambda}{NA}

\lambda: wave length
NA: Numerical Aperture

NA = n \cdot \sin \theta
K1: process constant [>0.25]

100nm
10μm
1μm

Recent trend of LSI scaling

Half pitch (nm)

2013 2015 2017 2019 2021 2023 2025 2027

- DRAM
- NAND Flash (2D)
- NAND Flash (3D)
- Logic-Metal
- Next memory (ReRAM, etc.)
- Immersion DP/MP
- Double patterning
- Quadruple patterning
- Octuple patterning

Scaling by immersion extension

ITRS 2013
Recent trend of LSI scaling

Cost effective is 1st priority
EUVL has potential of high resolution.

Resolution = \( \frac{\lambda}{\text{NA}} \)

\( \lambda \): exposure wavelength
\( \text{NA} \): Numerical Aperture
\( k_1 \): process constant [>0.25]

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Resolution \( \rightarrow \) less than 10 nm
### History of lithography potential solutions of ITRS

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<th>ArF</th>
<th>F2</th>
<th>ArF i</th>
<th>ArF HI</th>
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<th>MP</th>
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So, we wait for EUVL long time.
National project for EUVL in Japan


- 1990:
  - 1992~95: SORTEC (mask, illumination and process development by Nikon and Hitachi)

- 1995:
  - 1998~2006: ASET (process, mask and metrology)
  - 2001~10: MIRAI (mask metrology)
  - 2002~11: EUVA (source, exposure tool and optics metrology)

- 2000:
  - 2003~07: Leading (source)

- 2005:
  - 2006~11: Selete (full field scanner, mask metrology)

- 2010:
  - 2006 ASML (Full field scanner; ADT)
  - 2010~ ASML (Pre production tool; 3100)
  - 2013~ ASML (Production tool; 3300)

- 2015:
  - 2012~: EIDEC (mask metrology and resist)

- 2020:
  - 2020~?: ASML (High NA scanner)

- 30 years anniversary in 2016 ➔ HVM will start!?
Challenges of EUV lithography for HVM
## Focus area of EUV lithography

<table>
<thead>
<tr>
<th>2011 / 22hp</th>
<th>2012 / 22hp</th>
<th>2013 / 22hp</th>
<th>2014 / 16hp</th>
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<tr>
<td><strong>1.</strong> Long-term reliable source operation with 200 W at IF</td>
<td><strong>1.</strong> Long-term reliable source operation with a. 200 W at IF in 2014 b. 500 W-1,000 W in 2016</td>
<td><strong>1.</strong> Long-term reliable source operation with a. 125 W at IF in 2014 b. 250 W in 2015</td>
<td><strong>1.</strong> Reliable source operation with &gt; 75% availability – 125 W at IF in 1H / 2015 (at customer) – 250 W at IF in 1H / 2016 (HVM entry at customer)</td>
</tr>
<tr>
<td><strong>2.</strong> Mask yield &amp; defect inspection/review infrastructure</td>
<td><strong>2.</strong> Mask yield &amp; defect inspection/review infrastructure</td>
<td><strong>2.</strong> Defect free masks through lifecycle &amp; inspection/review infrastructure</td>
<td><strong>2.</strong> Resist resolution, sensitivity &amp; LER met simultaneously – Progress insufficient to meet 2015 introduction target</td>
</tr>
<tr>
<td><strong>3.</strong> Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td><strong>3.</strong> Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td><strong>3.</strong> Keeping mask defect free - Availability of pellicle mtg HVM req’t - Minimize defect adders during use</td>
<td><strong>3.</strong> Mask yield &amp; defect inspection/review infrastructure – Enable high yield defect free mask blank supply chain</td>
</tr>
<tr>
<td>• EUVL manufacturing integration</td>
<td>• EUVL manufacturing integration</td>
<td>4. Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td>4. Keeping mask defect free – Availability of pellicle mtg HVM req’t: need integrated industry strategy for solution – Minimize defect adders during use</td>
</tr>
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</table>

1st step for HVM

- Requirements for pilot production
  - Acceptable performance for pilot production
    - Throughput with source power of > 100 W
    - Tool availability more than 75 %
    - Lithographic performance (CDU, LWR, OL)
    - Process repeatability
  - Defectivity to keep available yield for device evaluation
    - Defectivity of mask blank and mask pattern
    - Pellicle ~ T = 85 %
    - Resist process defectivity
Source power for pilot production

• LPP(Laser Produced Plasma) source
  – **Current power ~100 W, availability ~ 55 %**
  – Challenges
    • More availability
    • Operational cost reduction
      – Debris mitigation
      – Droplet generator
      – Collector mirror

![Diagram](image-url)
EUV source power

Is it possible to improve availability and power at the same time?
RLS trade off of EUV resist

- **Resolution: target \( \leq 16 \) nm LS**
  - Resolution of EUV resist is not enough, higher \( k_1 \) (poorer) than ArF.
    - \( 14 \)nm LS(\( NA=0.33 \))~\( k_1=0.34 \)(CAR)~ worse LWR
    - \( 13 \)nm LS(\( NA=0.33 \))~ ~\( k_1=0.32 \)(non-CAR)~ lower sensitivity
  - LS pattern of ArF resist~ \( k_1=0.26 \), 2D pattern~ \( k_1=0.31 \)

<table>
<thead>
<tr>
<th>( NA )</th>
<th>( k_1 )</th>
<th>EUV resist (2D)</th>
<th>EUV resist (LS)</th>
<th>ArF resist (2D)</th>
<th>ArF resist (LS)</th>
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</table>
N7 Logic: Routed 2D semi-gridded Metal 1
36x38nm (PV x PH)

~20nm trench2trench separation

36nm PV

20nm T2L

38nm PH

~17nm trench

This example would require 4 exposures with 193 immersion – or one with 0.33NA EUVL

Conditions: NXE:3300B, annular illumination, 60nm resist, 40mJ/cm² dose
RLS trade off of EUV resist

- **LWR: target ≤ 3 nm**
  - Current level is >5 nm@ 16nm LS
  - Additional process can improve LWR of high frequency.
  - *It is very difficult to improve LWR of low frequency.*
  - *Etch resistance should be improved.*

- **Sensitivity: target ≤20mJ/cm²**
  - CAR: ~ 40 mJ/cm²
EUV resist

• It becomes harder to achieve RLS trade off for smaller CD.
  - **CAR:** LER / LWR
  - **Non-CAR:** Sensitivity (>60mJ/cm²)
  - **Etch resistance**

Example of resist pattern

[Graph showing optimum dose (mJ/cm²) vs. L&S hp (nm)]

→ Breakthrough of resist material
Paradigm shift to new platform
Imaging evaluation for $\leq 15$nm DRAM storage node layer

Preliminary results on a NXE:3300B

Dense CH – 20nm HP

Dense CH – 18nm HP

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<th>CD</th>
<th>FW CDU</th>
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$Dose \approx 37 \text{mJ/cm}^2$

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<tr>
<td>CH</td>
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$Dose \approx 49 \text{mJ/cm}^2$

Experimental conditions
- NA=0.33, sigma inner/outer=0.6/0.9 Quasar - 30

CDU $\leq 1.5$nm at $\sim 80$ W

Courtesy of ASML
# EUV Mask Infrastructure Readiness

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<td><strong>Mask Defect QA</strong></td>
<td>SEM + Litho. Simulation</td>
<td>SEM + Litho. Simulation</td>
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</table>

- **Green** indicates the process is ready.
- **Yellow** indicates the process is under development.
EUV pellicle

NXE Pellicle concept: particle free mounting/ de-mounting
Allowing multiple inspection schemes

Key features

- Reticle front side defect-free solution
  - protects reticle front side from fall-on defects
  - particle free material combination and mounting technology to prevent particle generation
  - additional particle suppression towards pattern area
- Designed for use in NXE scanner
  - pump down/vent cycles compatible
  - vacuum and H₂ environment compatible
  - meets outgassing requirements
  - no overlay impact, distortion-free mounting
- Compatible with standard EUV mask flow
  - concept supports any type of pattern mask inspection: optical, e-beam, and actinic; both at mask shop and fab
  - allows for reticle repel cycle

Courtesy of ASML
2\textsuperscript{nd} step for HVM

- Requirements for high volume production
  - Acceptable performance
    - Ultimate high throughput with > 250 W source
    - Tool availability more than 95 %
    - Lithographic performance (CDU, LWR, OL) with 250 W source i.e. higher scanning speed
    - Process repeatability and stability with 250 W source, i.e. higher temperature control
    - Defectivity to keep high yield for the real production
      - The requirement level depends on type of device and design
        - Pellicle: \( T > 90 \% \) (= 20\% loss of light intensity)
      - Need maximum continuous efforts for the lowest CoO
    - Cost down of consumable parts and materials
EUV source power

Next target: 500W

Current level: 80-100W

Future target 1kW@2020年～

1st target 250W, 125wph

Availability: 55%, 70%, 80%, 90%

DELAY

Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
Pattern shrink trend based on ITRS 2013

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<td>ReRAM</td>
<td>EUV(NA=0.33) Single</td>
<td>EUV(NA=0.33) DPT</td>
<td>EUV(NA=0.33) MPT</td>
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Single exposure by high NA EUV
EUV resist for high NA EUV

• RLS trade off
  – Difficult to overcome RLS trade off for smaller CD
  – More influence of shot noise in smaller CD. More dose will be required for smaller CD.
  – Resolution will become 1\textsuperscript{st} priority, so sensitivity will be the last priority.

• Etch resistance
  – Resist thickness is reducing with scaling. Etch resistance should be kept at same level as ArF resist.

• New platform materials
  – Nano-particle resist
  – Inorganic resist
  – \textbf{Need new idea for break through}!!
EUV scanner and source for high NA EUV

• High power source of 500 ~ 1000 W
  – Durability and heat treatment of all mirrors, mask and pellicle
  – Very high availability by short maintenance and longer lifetime of consumable parts
  – **XFEL is a candidate of the future source.**

• Scanner
  – Because high NA scanner will be very expensive, **higher throughput** and **ultimate availability** will be required strongly.
  – Smaller field size with 8X mask will lead high speed scanning stage in order to minimize the decrease of throughput.
  – Keeping 4X mask is the best way to achieve the highest TPT.
High power source

• **LPP**(Laser Produced Plasma)
  – **Current target:** 250 W
  – Scalability of LPP source to >> 250 W ??

• **EUV-FEL**(Free Electron Laser Laser)
  – No experience in semiconductor industry
  – Still in the conceptual stage for $\lambda = 13.5$ nm
Concerns for EUV-FEL

- Proof of concept; $\lambda=13.5$ nm / $>10$ kW
  - difficult to make a pilot system $\sim$ takes long time to build

- Availability for 365D/24H
  - Redundancy system

- Impact for wafer cost
  - FEL cost is expected to be lower than LPP.

- Electrical power consumption
  - FEL will be better than LPP.

- Facility size
  - Very large underground facilities ($>\sim100$ m)

- Timely readiness; long lead time items
  - Long term project management

- Coherence cause speckle noise and peak power cause damage
  - Need new idea for all reflective optics
There are many challenges for high power EUV-FEL. But nothing will be a show stopper, technically. Careful and sufficient optimization will be required.
Optics for high NA and high power

- Speckle noise due to **high coherence**
- Damage due to **high power EUV light** for all optics (e.g. beam splitter and transport system, ML mirror, mask and pellicle)

Beam splitter & transport system

- XFEL

Actual size ~100 m

10 scanners

Scanner

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High NA EUV trade-off: EUV optics

Countermeasure
1) Increasing CRA: Difficult
   Because of pattern shift in defocus due to mask 3D effect

2) Reduction ratio change from 1/4 to 1/6 ~ 1/8 with keeping CRA=6 deg.
   2-1) Increasing mask size to 9 inch: Difficult
       Because of the renewal of mask infrastructure
   2-2) Decreasing of exposure field size to 1/2 or 1/4
       Challenge for TPT (concern about CoO)

ASML proposal: “HF”
8X in scan direction
4X in other direction

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Maximizing throughput of high NA EUV

Limited by mechanical constraint of scanner (scanning speed, acceleration, etc.)

Source power / dose [W/(mJ/cm²)]

Throughput [W]

4X, FF
Maximizing throughput of high NA EUV

Degradation in HF (or QF) by increasing field number and mechanical constraint of scanner (scanning speed, acceleration, etc.)

Source power / dose [W/(mJ/cm²)]
Maximizing throughput of high NA EUV

Improved scanning stage (higher scanning speed and higher acceleration, etc.) But, not best solution!

Source power / dose \([W/(mJ/cm^2)]\)

Throughput \([\text{WPH}]\)
Maximizing throughput of high NA EUV

TPT Can be maximized by improved scanning stage with 4X + FF

Source power / dose [W/(mJ/cm²)]
Maximizing throughput of high NA EUV

High power source > 1kW for > 50mJ/cm²?

4X, FF, improved scan
How to realize 4X mask for high NA

Etched ML pattern has possibility for 4X FF mask.

Etched multilayer L/S pattern of 40 nm hp on mask (10 nm hp on wafer using 4X optics) is achieved.

→ Enabler of high NA, 4X full-field and 6 inch mask.
Lithography history

Resolution or CD

- Contact exposure
- DNQ / novolak resist
- G-line WL: 436nm
- High NA & shorter WL
- i-line 365nm
- KrF 248nm
- ArF 193nm
- ArF imm 193nm
- Computational lithography
- Double / multiple Patterning
- RET/ OPC
- LOGIC
- MEMORY

Resolution = k1 \( \frac{\lambda}{\text{NA}} \)

\( \lambda \): wave length
\( \text{NA} \): Numerical Aperture

\( \text{NA} = n \cdot \sin \theta \)

\( k1 \): process constant \( [>0.25] \)

- New resist?
- LPP source
- EUV(13.5nm)

Summary
Trend of EUV lithography

**EUV scanner**
- **Challenges**: Source power, CoO
- **Source** power:
  - 2012: 40W LPP
  - 2013: 125W LPP
  - 2014: 250W LPP
  - 2015: 500W
- **NA=0.25**
- **NA=0.33**
- **1st Target**

**EUV mask infra.**
- 2012: 16nm
- 2013: 11nm
- 2014: 11nm
- 2015: <11nm
- 2020: <11nm

**EUV resist**
- 2012: 16~13nm
- 2013: 11nm
- 2014: <6nm
- 2015: 0.26
- 2020: 0.26

**RLS trade-off**, Pattern collapse, Resist for high NA EUV

**Defectivity**, **Pattern placement error**, **Process stability**, **Metrology & inspection**, **Optimization of guide pattern design**

**ITRS**
- **Logic (node/hp)**
  - 20/40nm
  - 14/32nm
  - 10/28nm
  - 7/23nm
  - 5/18nm
- **NAND Flash memory**
  - 18nm
  - 17nm
  - 15nm
  - 14nm
  - 13nm
  - 12nm
- **ReRAM**
  - 12nm
  - 8nm

**High NA EUV**
- High power
- High NA EUV

**Magnification**
- <k1 factor

**Pellicle, Higher sensitivity for scaling, CoO**

**Trends**
- 2012: 16nm
- 2013: 11nm
- 2014: 11nm
- 2015: <6nm
- 2020: <6nm

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2015 International Workshop on EUV Lithography

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Summary

- EUVL will to be introduced into logic pilot production in near future.
  - Source power of > 100 W
  - Tool availability more than 75%

- More requirements for high volume production
  - Cost-effectiveness should be considered.
  - Ultimate high throughput with > 250 W source
  - Tool availability more than 95%
  - Breakthrough of EUV resist
  - Throughput can be maximized by high power source (> 1kW) and 4X full-field 6 inch mask with etched ML mask for high NA EUV.
Acknowledgment

The author would like to thank ASML